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**UTILITY  
PATENT APPLICATION  
TRANSMITTAL**

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No. 06192.0141.NPUS00

First Named Inventor or Application Identifier

Dong-Gyu KIM

Title Liquid Crystal Display

Express Mail Label No.

**APPLICATION ELEMENTS**

(See MPEP chapter 600 concerning utility patent application contents)

**ADDRESS TO:**

Assistant Commissioner for Patent

Box Patent Application

Washington, DC 20231

1. ☒ \*Fee Transmittal Form (Form PTO-1082)  
(Submit an original and a duplicate for fee processing)
2. ☒ Specification [Total Pages 36]  
(preferred arrangement set forth below)
- Descriptive title of the Invention
  - Cross References to Related Applications
  - Statement Regarding Fed sponsored R&D
  - Reference to Microfiche Appendix
  - Background of the Invention
  - Brief Summary of the Invention
  - Brief Description of the Drawings (if filed)
  - Detailed Description
  - Claims
  - Abstract of the Disclosure
3. ☒ Drawing(s) (35 USC 113) [Total Sheets 24]
4. ☐ Oath or Declaration [Total Pages ]
- a. ☐ Newly executed (original or copy)
- b. ☐ Copy from a prior application (37 CFR 1.63(d))  
(for continuation/divisional with Box 17 completed)  
[Note Box 5 below]
- i. ☐ **DELETION OF INVENTOR(S)**  
Signed statement attached deleting inventor(s) named  
in the prior application, see 37 CFR 1.63(d)(2) and  
1.33(b).
5. ☐ Incorporation By Reference (useable if Box 4b is checked)  
The entire disclosure of the prior application, from which a copy  
of the oath or declaration is supplied under Box 4b, is considered  
as being part of the disclosure of the accompanying application  
and is hereby incorporated by reference therein.

6. ☐ Microfiche Computer Program (Appendix)
7. Nucleotide and/or Amino Acid Sequence Submission  
(if applicable, all necessary)
- a. ☐ Computer Readable Copy
- b. ☐ Paper Copy (identical to computer copy)
- c. ☐ Statement verifying identity of above  
copies

**ACCOMPANYING APPLICATION PARTS**

8. ☐ Assignment Papers (cover sheet & document(s))
9. ☐ 37 CFR 3.73(b) Statement ☐ Power of  
(when there is an assignee) Attorney
10. ☐ English Translation Document (if applicable)
11. ☐ Information Disclosure ☐ Copies of IDS  
Statement (IDS)/PTO-1449 Citations
12. ☐ Preliminary Amendment
13. ☒ Return Receipt Postcard (MPEP 503) (Two)  
(should be specifically itemized)
14. ☐ \*Small Entity ☐ Statement filed in  
Statement(s) prior application,  
Status still proper  
and desired
15. ☒ Certified Copy of Priority Document(s)  
(if foreign priority is claimed)
16. ☐ Other:

\*NOTE FOR ITEMS 1 & 14 IN ORDER TO BE ENTITLED TO PAY SMALL ENTITY  
FEES, A SMALL ENTITY STATEMENT IS REQUIRED (37 CFR § 1.27), EXCEPT IF  
ONE FILED IN A PRIOR APPLICATION IS RELIED UPON (37 CFR § 1.28)

**17. If a CONTINUING APPLICATION, check appropriate box and supply the requisite information:**

☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No: /

Prior Application Information: Examiner:

Group/Art Unit:

**18. CORRESPONDENCE ADDRESS**

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Signature				Date	July 13, 2000

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**HOWREY SIMON ARNOLD & WHITE, LLP****Box No. 34****1299 Pennsylvania Avenue, N.W.****Washington, D.C. 20004-2402****(202) 783-0800**Attorney Docket No. 06192.0141.NPUS00COMMISSIONER FOR PATENTS  
Washington, D.C. 20231

Sir:

Transmitted herewith for filing is the patent application of

Inventors: Dong-Gyu KIM

For: **Liquid Crystal Display**

Enclosed are:

- ☒ 24 sheets of informal drawings (Figures 1-13, 14A-14B, 15A-15B, 16A-16B, 17A-17B, and 18-20, inclusive).  
☐ An assignment of the invention to \_\_\_\_\_

Form PTO-1595.

- ☒ certified copies of Korean Patent Application Nos. 99-28287, 99-48841, 99-67761.  
☐ An associate power of attorney.  
☐ A verified statement to establish small entity status under 37 CFR 1.9 and 37 CFR 1.27.  
☐ Executed Power of Attorney from Assignee  
☐ Executed Declaration for Patent Application.

The filing fee has been calculated as shown below:

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FOR	NO. FILED	NO. EXTRA
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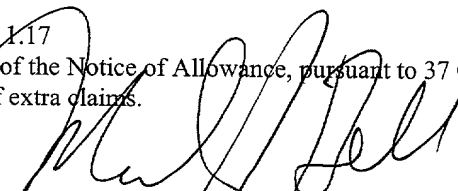
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☐ Any filing fees under 37 CFR 1.16 for presentation of extra claims.

Date

7/13/00
  
 Michael J. Bell (Reg. No. 38,604)



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July 13, 2000



Commissioner for Patents  
Washington, D.C. 20231

***Box Patent Application***

Re: U.S. Non-Provisional Utility Patent Application  
Application Serial No. **To Be Assigned**; Filed: July 13, 2000  
For: **Liquid Crystal Display**  
Inventor: **Dong-Gyu KIM**  
Our Ref: **06192.0141.NPUS00**

Sir:

The following documents are forwarded herewith for appropriate action by the U.S. Patent and Trademark Office:

1. U.S. Utility Patent Application entitled:  
**Liquid Crystal Display**  
and naming as inventor:  
**Dong-Gyu KIM**  
the application comprising:
  - a. A specification containing:
    - (i) **24** pages of description prior to the claims;
    - (ii) **11** pages of claims (Claims 1-51);
    - (iii) a one (1) page abstract;
  - b. 24 sheets of informal drawings: (Figures 1-13, 14A-14B, 15A-15B, 16A-16B, 17A-17B, and 18-20 inclusive); and
2. Form PTO-1082 (in duplicate);
3. Utility Patent Application Transmittal (PTO/SB/05);

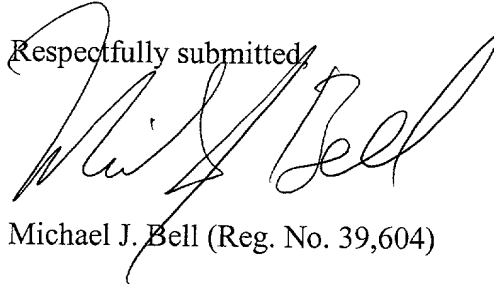
Assistant Commissioner for Patents  
July 13, 2000  
Page 2

4. Claim to Priority under 35 U.S.C. § 119(a)-(d);
5. Certified copies of Korean Patent Application Nos. 99-28287, 99-48841, 99-67761, filed July 13, 1999, November 5, 1999 and December 31, 1999, priority of which is hereby claimed;
6. Our check No. 331055 for \$1,404.00 to cover:  
\$690.00 filing fee for patent application;  
\$714.00 fee for excess claims; and
7. Two (2) return postcards.

It is respectfully requested that, of the two attached postcards, one be stamped with the filing date of these documents and returned to our courier, and the other, prepaid postcard, be stamped with the filing date and unofficial application number and returned as soon as possible.

This patent application is being submitted under 37 C.F.R. § 1.53(b) without Declaration.

Respectfully submitted,



Michael J. Bell (Reg. No. 39,604)

Enclosures

# LIQUID CRYSTAL DISPLAY

## BACKGROUND OF THE INVENTION

### **(a) Field of the Invention**

5           The present invention relates to a liquid crystal display and, more particularly, to a liquid crystal display which bears uniform brightness characteristic over the entire screen area without leakage of light.

### **(b) Description of the Related Art**

10           Generally, a liquid crystal display has an upper substrate with a common electrode and color filters (usually called the “color filter substrate”), a lower substrate with thin film transistors and pixel electrodes (usually called the “TFT array substrate”), and a liquid crystal layer sandwiched between the color filter substrate and the TFT array substrate. Different electrical potentials are applied to the pixel electrodes and the common electrode while forming electric fields to change the liquid crystal molecule orientation. In this way, the light transmission is controlled to display picture images.

15           In such a liquid crystal display, with only a TFT attached to it, the charge applied to switch the liquid crystal leaks away in a brief time after a signal arrives. Therefore, it is necessary to connect an additional capacitor to the liquid crystal so that the liquid crystal is able to retain the charge associated with the first signal until a second signal is received.

20           For example, a capacitance may be conferred on a liquid crystal by using an adjacent gate electrode line.

Each pixel electrode overlaps over the previous gate line with an insulating layer interposed to form a storage capacitance  $C_{st}$ . The pixel electrode faces the common electrode with a liquid crystal layer interposed to form a liquid crystal capacitance  $C_{lc}$ . Furthermore, a parasitic capacitance  $C_{gd}$  is formed between a gate electrode and a drain electrode.

The voltage applied between each pixel electrode and the common electrode changes at 60Hz (60 frames per second). Within one frame, pulses of  $V_{on}$  are applied to sequentially turn on TFTs from the first gate line to the last gate line. In case the  $V_{on}$  pulse is applied to a particular gate line, off-voltages  $V_{off}$  are applied to the other gate lines. When the voltage applied to the common electrode  $V_{com}$  is set to 5V, the on-voltage  $V_{on}$  becomes to be about 20V, and the off-voltage  $V_{off}$  to be about -7V. When the on-voltage  $V_{on}$  is applied to a particular gate line, the TFTs positioned at that line are in an on-state, and the picture signal voltages applied to the data lines are transmitted to the pixel electrodes. In contrast, when the off-voltage  $V_{off}$  is applied to the TFTs at the particular gate line while applying  $V_{on}$  to the previous gate line, the electric potential  $V_g$  of the previous gate line is elevated by 27V from -7V to 20V. At this time, the electric potential of the pixel electrode  $V_p$  is also increased. The amount of increased potential of the pixel electrode  $\Delta V_p$  can be expressed by the following equation:

$$\Delta V_p = [C_{st}/(C_{st}+C_{lc}+C_{gd}+\text{other parasitic capacitance})] \times \Delta V_g (=27V).$$

At this time, the liquid crystal capacitance  $C_{lc}$  as a function of voltage difference between  $V_{com}$  and  $V_p$  as well as the parasitic capacitance  $C_{gd}$  are

varied together. Thereafter, when the previous gate line is shifted from Von to Voff, the electric potential of the pixel electrode  $V_p$  returns to the initial state, but not the liquid crystal capacitance  $C_{lc}$  and the parasitic capacitance  $C_{gd}$  due to voltage dependence thereof. As such a variation in electrical potentials of the pixel electrodes at the second to last gate lines are made in the same pattern, the pixel electrode portions at the second to last gate lines bears uniform brightness at the same gray scale. However, since the pixel electrodes at the first gate line have no previous gate line, the electrical potentials of those electrodes change in different manner and the brightness becomes different in the same gray scale. As the brightness at the first gate line portion is usually brighter compared to other gate line portions, the picture images displayed at that portion disturbs the human eye.

In order to solve such a problem, the technique of adding a storage capacitor line G0 and connecting it to the second gate line G2 or the last gate line  $G_m$  has been proposed. However, when the G0 line is connected to the G2 line, the integrated circuit (IC) for driving the G2 line should be also employed for driving the G0 line, resulting in shortage in driving current. Accordingly, the second gate line portion becomes much brighter than other gate line portions at a normally white mode. This phenomenon becomes serious as the electric load applied to each gate line becomes greater with the trend of high definition and increased screen size. In contrast, when the G0 line is connected to the  $G_m$  line, complicated wiring via printed circuit boards (PCBs) should be made to interconnect the G0 line and the  $G_m$  line, and the

first and the last gate line portions differs in brightness from the other gate line portions.

In the meantime, the TFT array substrate usually has a size larger than the color filter substrate. In this connection, when assembled, the periphery of the TFT array substrate without the corresponding black matrix portion is exposed to the outside so that light leaks at the exposed portion.

### **SUMMARY OF THE INVENTION**

It is an object of the present invention to provide a liquid crystal display which bears good picture quality with uniform brightness characteristic over the entire screen area.

It is another object of the present invention to provide a liquid crystal display which effectively prevents light leakage without generating short circuits.

These and other objects may be achieved by employing in a liquid crystal display light interception patterns. Alternatively, a liquid crystal display may have a black matrix with openings of different sizes depending on the pixel positions. A manufacturing method is also disclosed.

According to one aspect of the present invention, the liquid crystal display includes first and second insulating substrates facing to each other, and a liquid crystal injected into the gap between the first and second substrates. A plurality of gate lines is formed at the first substrate to transmit scanning signals, and data lines cross over the gate lines to transmit picture signals. Pixels are demarcated by the gate lines and the data lines. The gate lines demarcate the pixels into rows, and the data lines demarcate the pixels into



columns. A black matrix defines each pixel, and a pixel electrode is formed at each pixel. A storage capacitor line is formed at the first substrate parallel to the gate line, and overlapped with the pixel electrodes at the first pixel row. Storage capacitors are formed between the pixel electrodes and the previous gate lines as well as between the pixel electrodes and the storage capacitor line. A gate-off voltage or a common electrode voltage is applied to the storage capacitor line. Each pixel at the first pixel row with the storage capacitor formed between the corresponding pixel electrode and the storage capacitor line has an opening ratio different from that of the pixels at the other pixel rows. The opening ratio of the first pixel row is established to be 60-80% of the opening ratio of the other pixel rows.

The opening ratio is made different by forming a light interception pattern at each pixel of the first pixel row, or by changing opening volumes of the black matrix. The light interception pattern may be formed at the same layer as the data line or the gate line with the same material.

A gate-off line is formed at the first substrate to transmit a gate-off voltage, and the gate-off line and the storage capacitor line are formed at the same layer as the gate line. The gate-off line and the storage capacitor line are electrically connected to each other via a connection member, and the connection member is formed at the same layer as the data line or the pixel electrode.

In the above structure, uniform brightness over the entire screen area can be ensured.

According to another aspect of the present invention, the liquid crystal display includes a first insulating substrate, and a gate line assembly formed at the first insulating substrate. The gate line assembly has a plurality of gate lines, gate electrodes branched from the gate lines, and gate pads connected to the gate lines to transmit scanning signals thereto. First light interception patterns are isolated from the gate line assembly. A gate insulating layer covers the gate line assembly and the first light interception patterns. A semiconductor layer is formed on the gate insulating layer, and an ohmic contact layer is formed on the semiconductor layer. A data line assembly is formed on the semiconductor layer and the gate insulating layer. The data line assembly has a plurality of data lines crossing over the gate lines while forming pixel areas, source electrodes branched from the data lines, drain electrodes positioned opposite to the source electrodes while centering around the gate electrodes, and data pads connected to the data lines to transmit picture signals thereto. The pixel areas collectively forms a display area. Second light interception patterns are isolated from the data line assembly. A protective layer covers the data line assembly and the second light interception patterns while forming first to third contact holes exposing the gate pad, the data pad and the drain electrode, respectively. Pixel electrodes are connected to the drain electrodes via the third contact hole. A subsidiary gate pad covers each gate pad via the first contact hole, and a subsidiary data pads covers each data pad via the second contact hole.

A second insulating substrate faces the first substrate, and color filters

are formed at the second substrate while corresponding to the pixel areas. A black matrix is formed at the second substrate while surrounding the color filters, and a common electrode covers the color filters and the black matrix. A sealer seals the first and second substrates together.

5           The first and second light interception patterns are positioned outside of the display area such that they are overlapped with the black matrix, but not with the gate and data lines, and the sealer.

In the above structure, possible light leakage can be prevented with the light interception patterns without generating short circuits.

#### **BRIEF DESCRIPTION OF THE DRAWINGS**

10           A more complete appreciation of the invention, and many of the advantages thereof, will be readily apparent as the same becomes better understood by reference to the following detailed description when considered in conjunction with the accompanying drawings in which like reference symbols  
15           indicate the same or the similar components, wherein:

Fig. 1 is a plan view of a liquid crystal display according to a first preferred embodiment of the present invention;

Fig. 2 is a cross sectional view of the liquid crystal display taken along the II-II' line of Fig. 1;

20           Fig. 3 is another plan view of the liquid crystal display shown in Fig. 1 illustrating the wiring structure;

Fig. 4 is a circuit diagram of the liquid crystal display shown in Fig. 1;

Fig. 5 is a plan view of a liquid crystal display with a black matrix

according to a second preferred embodiment of the present invention;

Fig. 6 is a cross sectional view of the liquid crystal display taken along the VI-VI' line of Fig. 5;

Fig. 7 is a plan view of the black matrix shown in Fig. 5;

5 Fig. 8 is a plan view of a liquid crystal display according to a third preferred embodiment of the present invention;

Fig. 9 is a circuit diagram of the liquid crystal display shown in Fig. 8;

Fig. 10 is a plan view of a liquid crystal display according to a fourth preferred embodiment of the present invention;

10 Fig. 11 is another plan view of the liquid crystal display shown in Fig. 10 illustrating the wiring structure;

Fig. 12 is a cross sectional view of the liquid crystal display taken along the XII-XII' line of Fig. 11;

15 Fig. 13 is a cross sectional view of the liquid crystal display taken along the XIII-XIII' line of Fig. 11;

Figs. 14A to 17B are views sequentially illustrating the steps of processing the liquid crystal display shown in Fig. 10;

Fig. 18 is a plan view of a liquid crystal display according to a fifth preferred embodiment of the present invention;

20 Fig. 19 is a cross sectional view of the liquid crystal display taken along the XIX-XIX' line of Fig. 18; and

Fig. 20 is a cross sectional view of the liquid crystal display taken along the XX-XX' line of Fig. 18.

## **DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS**

Preferred embodiments of this invention will be explained with reference to the accompanying drawings.

Fig. 1 is a plan view of a liquid crystal display according to a first preferred embodiment of the present invention where one pixel area of the first pixel row is illustrated, and Fig. 2 is a cross sectional view of the liquid crystal display taken along the II-II' line of Fig. 2. The liquid crystal display according to the present invention has a basic structure where a liquid crystal layer is sandwiched between upper and lower substrates with a plurality of pixel areas at different pixel rows, and the following description will be made with respect to one pixel area at the first pixel row.

As shown in the drawings, the lower substrate 10 is overlaid with a first gate line 22 proceeding in the horizontal direction, a gate electrode 26 branched perpendicularly from the first gate line 22 and a storage capacitor line G0 proceeding parallel to the first gate line 22. A gate insulating layer 30 is formed on the gate line 22, the gate electrode 26, and the storage capacitor line G0. A semiconductor layer 40 is formed on the gate insulating layer 30 over the gate electrode 26, and a data line 62 is formed on the gate insulating layer 30 while crossing perpendicularly over the first gate line 22 and the storage capacitor line G0. A source electrode 65 is branched perpendicularly from the data line 62. A drain electrode 66 is positioned at the same plane as the source electrode 65 opposite thereto while centering around the gate electrode 26. The source and drain electrodes 65 and 66 are placed over the

semiconductor layer 40 by interposing ohmic contact layers 55 and 56.

Of course, the storage capacitor line G0 may be referred to as the first gate line if it functions as an electrode part of a storage capacitor for the first pixel row.

5 A light interception pattern 67 is centrally formed at the pixel area with the same plane as the data line 62, the source electrode 65 and the drain electrode 66. A protective layer 70 is formed on the data line 62, the source electrode 65 and the drain electrode 66 with a contact hole 81 exposing the drain electrode 66. A pixel electrode 80 is formed on the protective layer 70, and connected to the drain electrode 66 via the contact hole 81. The pixel electrode 80 is formed with a transparent material such as indium tin oxide (ITO), and partially overlapped with the storage capacitor line G0. Each pixel area is demarcated by the two data lines 62 crossing over the neighboring two gate lines, and the pixel electrode 80 covers the entire pixel area.

10 A black matrix 91 and color filters (not shown) are formed on the upper substrate 90 such that they face the lower substrate 10. The black matrix 91 is formed of opaque material that can prevent light leakage. It also defines each pixel area. A common electrode 92 is formed on the black matrix 91 and the color filters. It covers the entire upper substrate 90. Alternatively, the black matrix 91 and the color filters may be formed at the lower substrate 10.

20 In the above pixel structure, the pixel electrodes 80 at the first pixel row overlap the storage capacitor line G0 to form a desired storage capacitance.

On the other hand, the pixel electrodes 80 of the second to the last pixel rows overlap the previous corresponding gate lines 22 respectively.

The first pixel row has an opening ratio lower than that of the other pixel rows due to the presence of the light interception patterns 67.

5        The light interception pattern 67 may be formed either at the same layer as the data line 62, the source electrode 65 and the drain electrode 66, or at the same layer as the gate line 22 and the gate electrode 26.

10        As shown in Fig. 3, when the lower substrate 10 is combined with the upper substrate 90, the periphery of the lower substrate 10 is exposed to the outside because it is larger than the upper substrate 90. Gate signal transmission films 28 are arranged at the exposed portion of the lower substrate 10 in the longitudinal direction of the data lines 62. Each gate signal transmission film 28 is provided with a gate driving integrated circuit 27. The gate driving integrated circuit 27 is electrically connected to the gate lines 22, and outputs gate driving signals. Data signal transmission films 68 are arranged at the exposed portion of the lower substrate 10 in the longitudinal direction of the gate lines 22. Each data signal transmission film 68 is provided with a data driving integrated circuit 67. The data driving integrated circuit 67 is electrically connected to the data lines 62, and outputs data driving signals. Furthermore, a printed circuit board 12 for driving the liquid crystal display is connected to the data signal transmissions 68.

20        Meanwhile, a common electrode wire 71 for applying the common electrode voltage Vcom to the common electrode 92, a gate-on wire 72 for

applying the on-voltage  $V_{on}$  to the TFTs, and a gate-off wire for applying the off-voltage  $V_{off}$  to the TFTs are formed on the edge portion of the lower substrate 10 between the gate signal transmission film 28 and the data signal transmission film 68. Additional wires for transmitting carry-in or gate-clock signals may be further provided.

As shown in Figs. 3 and 4, the storage capacitor line G0 at the first pixel row is connected to the gate-off wire 73 via a connection member such that the gate-off voltage  $V_{off}$  is transmitted thereto. It is preferable that the common electrode wire 71, the gate-on wire 72 and the gate-off wire 73 are formed at the same layer as the storage capacitor line G0 and the gate lines 22 with the same material. The connection member 77 is formed at the same layer as the data lines 62 or the pixel electrodes 80 with the same material. The protective layer 70 or the gate insulating layer 30 has a contact hole that receives the connection member 77.

Because the substrate 10 has the wires 71 to 73 that transmit appropriate signals to the gate driving integrated circuit 27, a connector that interconnects a gate printed circuit board and a data printed circuit board may be eliminated. Furthermore, as in this preferred embodiment, only the data printed circuit board may be used without the gate printed circuit board.

The gate driving integrated circuit 27 and the data driving integrated circuit 67 may be directly mounted onto the lower substrate 10.

As described above, the opening ratio of the first pixel row is lower to compensate a possible increase in brightness at the first pixel row when



applying the off-voltage  $V_{off}$  to the storage capacitor line G0. Furthermore, even though slight darkness is present at the first pixel row portion due to the presence of the light interception patterns 67, it is not unpleasant to the eye, producing good picture quality.

5 It turns out that the optimal opening ratio of the first pixel row lies in the range of 60-80% of the other pixel rows. Of course, such a value may be slightly different depending upon the factors such as light transmission, Clc, or Cst.

10 In this way, the resulting liquid crystal display can bear good picture quality by compensating brightness differences with a simplified wiring structure.

Alternatively, in order to reduce the opening ratio of the first pixel row, the opening portions of the black matrix 91 at the first pixel row may be reduced to be smaller than those of the black matrix 91 at the other pixel rows.

15 Fig. 5 is a plan view of a liquid crystal display according to a second preferred embodiment of the present invention where one pixel area at the first pixel row is illustrated, and Fig. 6 is a cross sectional view of the liquid crystal display taken along the VI-VI' line of Fig. 5. In this preferred embodiment, other components and structures of the liquid crystal display are the same as those  
20 related to the first preferred embodiment except that the first pixel row's opening portions of the black matrix 91 are different in lengths from the other pixel rows and that the light interception patterns 67 is eliminated.

As shown in Fig. 7, the opening portions 93 of the black matrix 91 at

the first pixel row are designed to have a smaller length than the opening portions 94 at the other pixel rows to reduce the opening ratio of the first pixel row. That is, the opening portions 94 of the black matrix 91 at the second to last pixel rows have a width X and a length Y while being spaced apart from each other with a distance S on the row by row basis. However, the opening portions 93 of the black matrix 91 at the first pixel row have a length Y-a to be 60 to 80% of the length Y of the other opening portions 94.

The structure where only the length of the opening portions 93 of the black matrix 91 at the first pixel row becomes decreased with a uniform width can produce better picture images. Of course, it is possible that the width and length of the opening portions 93 of the black matrix 91 at the first pixel row are all decreased to reduce the opening ratio at those portions.

Figs. 8 and 9 illustrate a liquid crystal display according to a third preferred embodiment of the present invention. In this preferred embodiment, other components and structures of the liquid crystal display are the same as those related to the second preferred embodiment except that the common electrode voltage Vcom is applied to the storage capacitor electrode G0 at the first pixel row, and the opening width and length of the black matrix 91 at the first pixel row are all designed to be shorter than those of the black matrix 91 at the other pixel rows.

Fig. 10 is a plan view of a liquid crystal display according to a fourth preferred embodiment of the present invention where a TFT array substrate 100 and a color filter substrate 110 are assembled via a sealer 3. Since the

TFT array substrate 100 is larger than the color filter substrate 110, it is partially exposed to the outside.

As shown in Fig. 10, a plurality of gate lines 200 are formed at the TFT array substrate 100 in the horizontal direction, and gate pads 230 are connected to the end portions of the gate lines 200. A plurality of data lines 610 are formed at the TFT array substrate 100 in the vertical direction, and data pads 640 are connected to the end portions of the data lines 610.

A plurality of pixel areas P are existent at the TFT array substrate 100. Each pixel area P is defined by the two data lines 610 crossing over the neighboring gate lines 200, and a display area A can be indicated by the sum of the pixel areas P. A sealer 3 externally surrounds the display area A.

Color filters CF are formed at the color filter substrate 110 such that each color filter CF faces the corresponding pixel area of the TFT array substrate 100. A black matrix BM surrounds the color filters CF such that it can prevent light leakage at the region between the neighboring pixel areas. As indicated in Fig. 10 with the solid line 2, the peripheral portion of the black matrix BM is placed inside the peripheral portion of the color filter substrate 110 while being positioned outside the sealer 3.

In the above structure, lights tend to leak at the region B between the gate and data pads 230 and 640 and the black matrix BM. In order to prevent such a light leakage, light interception patterns 250 and 650 are formed at that region B such that they do not overlap the gate and data lines 200 and 610, and the gate and data pads 230 and 640. Furthermore, the light interception

patterns 230 and 640 should not be overlapped with the sealer 3, but may be overlapped with the black matrix BM.

Alternatively, the color filters CF and the black matrix BM may be formed at the TFT array substrate 100.

5 Fig. 11 is an amplified view of the C portion of the liquid crystal display shown in of Fig. 10. Fig. 12 is a cross sectional view of the liquid crystal display taken along the XII-XII' line of Fig. 11. Fig. 13 is a cross sectional view of the liquid crystal display taken along the XIII-XIII' line of Fig. 11.

10 As shown in the drawings, the TFT array substrate 100 is overlaid with a gate line assembly, and first light interception patterns 250. The gate line assembly includes a plurality of gate lines 200, gate electrodes 210 branched from the gate lines 200, and gate pads 230 connected to the end portions of the gate lines 200 to receive scanning signals from the outside and transmit them to the gate lines 200. The gate line assembly and the first light interception patterns 250 are placed on the same plane, and formed together with a conductive metallic material such as aluminum (Al), aluminum alloy, molybdenum (Mo), molybdenum-tungsten alloy (MoW), chrome (Cr), and tantalum (Ta).

15 The gate line assembly and the first light interception patterns 250 may be formed either with a single layer or with double or more layers. In the case of the double-layered structure, it is preferable that one layer is formed with a material having a low resistance while the other layer being formed with a material having a good contact characteristic. For instance, two layers based

on chrome and aluminum or based on aluminum and molybdenum may be provided for the double-layered structure.

The gate line assembly and the first light interception patterns 250 are covered by a gate insulating layer 300. The gate insulating layer 300 may be formed with silicon nitride.

A semiconductor layer 410 is formed on the gate insulating layer 300, and two separate ohmic contact layers 520 and 530 are formed on the semiconductor layer 410 while centering around the gate electrode 210. The semiconductor layer 410 may be formed with amorphous silicon, and the ohmic contact layers 520 and 530 with amorphous silicon into which n-type impurities such as phosphorus (P) are doped.

A data line assembly and second light interception patterns 650 are formed on the ohmic contact layers 520 and 530 and the gate insulating layer 300. The data line assembly includes a plurality of data lines 610, source electrodes 620 branched from the data lines 610, drain electrodes 630 positioned opposite to the source electrodes 620 while centering around the gate electrode 210, and data pads 640 connected to the end portions of the data lines 610 to receive picture signals from the outside and transmit them to the data lines 610. The data line assembly and the second light interception patterns 650 are placed on the same plane, and formed together with a conductive metallic material such as aluminum (Al), aluminum alloy, molybdenum (Mo), molybdenum-tungsten alloy (MoW), chrome (Cr), and tantalum (Ta).

As in the gate line assembly and the first light interception patterns 250, the data line assembly and the second light interception patterns 650 may be formed either with a single layer or with double or more layers.

The second light interception patterns 650 are positioned at the region between the gate pads 230 and the display area A as well as between the neighboring gate lines 200 such that they are not overlapped with the gate lines 200 and the gate pads 230. Likewise, the first light interception patterns 250 are positioned at the region between the data pads 640 and the display area A as well as between the neighboring data lines 610 such that they are not overlapped with the data lines 610 and the data pads 640.

A protective layer 700 is formed on the data line assembly, the second light interception patterns 650, the semiconductor layer 410, and the gate insulating layer 300. The protective layer 700 may be formed with silicon nitride. The protective layer 700 has a contact hole 730 exposing the gate pad 230 together with the gate insulating layer 300, a contact hole 740 exposing the data pad 640, and a contact hole 720 exposing the drain electrode 630.

Pixel electrodes 820, subsidiary gate pads 830, and subsidiary data pads 840 are formed on the protective layer 700 with a transparent material such as indium tin oxide (ITO).

Each pixel electrode 820 is connected to the drain electrode 630 via the contact hole 720. The subsidiary gate pad 830 and the subsidiary data pad 840 are connected to the gate pad 230 and the data pad 640 via the contact holes 730 and 740, respectively. The subsidiary gate and data pads 830 and

840 are provided to enhance adhesion between the gate and data pads 230 and 640 and the external circuits, and to protect the gate and data pads 230 and 640.

An alignment layer 900 is formed on the protective layer 700 and the pixel electrodes 820. In order to align the liquid crystal molecules, the alignment layer 900 may be surface-treated through rubbing or light illumination.

In the meantime, the color filter substrate 110 is overlaid with a black matrix 710, and color filters 750 surrounded by the black matrix 710.

An ITO-based common electrode 810 is formed on the black matrix 710 and the color filters 750, and an alignment layer 910 is formed on the common electrode 810.

The TFT array substrate is assembled with the color filter substrate 110 via a sealer 3, and a liquid crystal LC is injected into the gap between the substrates.

As shown in Figs. 10 to 13, the borderline of the color filter substrate 110 is indicated by the reference numeral 1, and the borderline of the black matrix 710 indicated by the reference numeral 2. The sealer 3 is positioned outside of the display area A, and the borderline 2 of black matrix 710 is disposed between the borderline 1 of the color filter substrate 110 and the sealer 3.

In view of alignment errors, the first light interception patterns 250 are spaced apart from the data lines 610 by a minimum distance a, and the second

light interception patterns 650 are spaced apart from the gate lines 200 by a minimum distance e. Furthermore, the first light interception patterns 250 are spaced apart from the data pads 640 by a reasonable distance b such that they are not overlapped with the data pads 640 as well as TCPs attached thereto in a reliable manner, and the second light interception patterns 650 are spaced apart from the gate pads 230 by a distance f. In addition, the first light interception patterns 250 are spaced apart from the sealer 3 by a distance c, and the second light interception patterns 650 are spaced apart from the sealer 3 by a distance g. As it is desirable that the first and second light interception patterns 250 and 650 do not have a gap with the black matrix 710, they are overlapped with the black matrix 710 by a span d and h in view of the alignment errors.

In case the first and second light interception patterns 250 and 650 are overlapped with the gate and data lines 200 and 610, short circuit may occur between them. Furthermore, in case the first and second light interception patterns 250 and 650 are overlapped with the sealer 3, short circuit may also occur between them when the sealer 3 is compressed for the sealing purpose. In the above structure, even though a small gap exists between the light interception patterns 250 and 650 and the gate and data lines 200 and 610, only negligible amount of light may leak there.

Such light interception patterns 250 and 650 may be also applied to in-plane switching (IPS) type liquid crystal displays where the common electrode and the pixel electrodes are formed at the TFT array substrate, and super



twisted nematic (STN) liquid crystal displays where stripe-shaped electrodes cross over at the two substrates without TFTs.

Figs. 14A to 17B sequentially illustrate the steps of processing the TFT array substrate on a layer by layer base.

5 As shown in Figs. 14A and 14B, a gate line assembly 200, 210 and 230, and first light interception patterns 250 are formed on an insulating substrate 100 through deposition and a first photolithography process.

10 Thereafter, as shown in Figs. 15A and 15B, a gate insulating layer 300, a semiconductor layer 410 and an ohmic contact layer 510 are sequentially deposited onto the substrate 100, and the ohmic contact layer 510 and the semiconductor layer 410 are patterned through a second photolithography process.

15 As shown in Figs. 16A and 16B, a data line assembly 610, 620, 630 and 640, and second light interception patterns 650 are formed through deposition and a third photolithography process. Thereafter, the portion of the ohmic contact layer 510 exposed between the source electrode 620 and the drain electrode 630 is removed such that the ohmic contact layer 510 is separated into two portions 520 and 530 to expose the semiconductor layer 410.

20 As shown in Figs. 17A and 17B, a protective layer 700 is deposited onto the substrate 100, and patterned through a fourth photolithography to form contact holes 720, 730 and 740.

Then, as shown in Figs. 12 and 13, pixel electrodes 820, subsidiary

gate pads 830, and subsidiary data pads 840 are formed at the substrate 100 through deposition and a fifth photolithography process. Thereafter, an alignment layer 900 is formed at the substrate 100.

The TFT array substrate 100 is then assembled with the color filter substrate 110 via a sealer 3, and a liquid crystal LC is injected into the gap between the substrates 100 and 110 to complete a liquid crystal panel. In case the alignment layer 900 of the TFT array substrate 100 overlaps the sealer 3, the overlapped portion of the alignment layer 900 is set to be 1/5 of the width of the sealer 3.

Thereafter, semiconductor circuits are mounted onto the liquid crystal panel.

First, an anisotropic conductive film (not shown) is formed at the exposed portion of the TFT array substrate 100 while covering the subsidiary gate and data pads 830 and 840, and TCPs with semiconductor circuits are arranged at the TFT array substrate 100, and thermal-compressed. In this case, the subsidiary pads 830 and 840 are electrically communicated with the TCPs via conductive balls contained in the anisotropic conductive film. This distance of b and f between the light interception patterns 250 and 650 and the pads 230 and 640 prevents possible short circuit via the conductive balls between the light interception patterns 250 and 650 and the subsidiary pads 830 and 840 during the thermal-compression.

Figs. 18 to 20 illustrate a liquid crystal display according to a fifth preferred embodiment of the present invention. In this preferred embodiment,

other components and structures of the liquid crystal display are the same as those related to the fourth preferred embodiment except that ohmic contact layers 520, 530 and 550 and semiconductor layers 410 and 450 are positioned under a data line assembly 610, 620, 630 and 640, and second light interception patterns 650. The shape of the ohmic contact layers 520, 530 and 550 is the same as that of the data line assembly 610, 620, 630 and 640 and the second light interception patterns 650. The shape of the semiconductor layers 410 and 450 is the same as that of the data line assembly 610, 620, 630 and 640 and the second light interception patterns 650 except the portions between the source electrodes 620 and the drain electrodes 630.

The fabrication process for the TFT array substrate is based on the four-mask photolithography.

First, a gate line assembly 200, 210 and 230 and first light interception patterns 250 are formed on an insulating substrate 100 through deposition and a first photolithography process. Thereafter, a gate insulating layer 300 is deposited onto the gate line assembly 200, 210 and 230 and the first light interception patterns 250 while covering them. Semiconductor layers 410 and 450, ohmic contact layers 520, 530 and 550, and a data line assembly 610, 620, 630 and 640 are sequentially deposited, and patterned through a second photolithography process. A protective layer 700 is deposited onto the substrate 100, and patterned through a third photolithography process to thereby form contact holes 720, 730 and 740. Thereafter, pixel electrodes 820, subsidiary gate pads 830 and subsidiary data pads 840 are formed at the

substrate 100 through deposition and a fourth photolithography process. Finally, an alignment layer is formed at the substrate 100.

In the second photolithography process, a photoresist film is deposited onto the conductive layer for the data line assembly, and patterned through a mask differentiated in light transmission. The exposed portion of the conductive layer is removed while exposing the underlying ohmic contact layer. The exposed portion of the ohmic contact layer and the underlying semiconductor layer are etched, and the portion of the conductive layer between the source and drain electrodes 620 and 630 is removed. Thereafter, the exposed portion of the conductive layer between the source and drain electrodes 620 and 630 and the underlying ohmic contact layer are etched together. In this way, the semiconductor layers 410 and 450, the ohmic contact layers 520, 530 and 550, the data line assembly 610, 620, 630 and 640, and the second light interception patterns 650 are formed at the substrate 100.

In the resulting liquid crystal display, light interception patterns are provided at the TFT array substrate, and spaced apart from the electrode components of lines, pads, and a sealer so that leakage of light and short circuit can be effectively prevented.

While the present invention has been described in detail with reference to the preferred embodiments, those skilled in the art will appreciate that various modifications and substitutions can be made thereto without departing from the spirit and scope of the present invention as set forth in the appended claims.

**WHAT IS CLAIMED IS:**

1. A liquid crystal display, comprising:

a first insulating substrate;

5 a plurality of gate lines formed at the first substrate to transmit scanning signals;

a plurality data lines crossing over the gate lines to transmit picture signals;

a second insulating substrate facing the first substrate;

10 a liquid crystal layer injected into the gap between said first insulating substrate and said second insulating substrate;

a pixel demarcated by the gate lines and the data lines, the gate lines demarcating the pixels into rows, and the data lines demarcating the pixels into columns;

15 a black matrix defining each pixel;

a pixel electrode formed at each pixel; and

a storage capacitor formed between said pixel electrode and the previous gate line;

wherein an opening ratio of each pixel at the first pixel row is different from the opening ratio of the pixels at the other pixel rows.

20 2. The liquid crystal display of claim 1, wherein the opening ratio of the first pixel row is lower than the opening ratio of the other pixel rows.

3. The liquid crystal display of claim 2, wherein the difference in the opening ratio is made by differentiating an opening area of the black matrix.

4. The liquid crystal display of claim 3, wherein the black matrix is formed at the second substrate.

5. The liquid crystal display of claim 2, wherein the difference in the opening ratio is made by forming a light interception pattern at each pixel of the first pixel row.

6. The liquid crystal display of claim 5, wherein the light interception pattern is formed at the same layer as the data line with the same material.

7. The liquid crystal display of claim 5, wherein the light interception pattern is formed at the same layer as the gate line with the same material.

8. The liquid crystal display of claim 2, wherein the opening ratio of the first pixel row is designed to be 60-80% of the opening ratio of the other pixel rows.

9. A liquid crystal display, comprising:  
a first insulating substrate;  
a plurality of gate lines formed at the first substrate to transmit scanning signals;  
a plurality of data lines crossing over the gate lines to transmit picture signals;  
a second insulating substrate facing the first substrate;  
a liquid crystal layer injected into the gap between said first insulating substrate and said second insulating substrate;

a pixel demarcated by the gate lines and the data lines, the gate lines demarcating the pixels into rows, and the data lines demarcating the pixels into columns;

a black matrix defining each pixel;

5 a pixel electrode formed at each pixel;

a storage capacitor line formed on said first insulating substrate parallel to the gate line, the storage capacitor line overlapping the pixel electrodes at the first pixel row;

10 a first storage capacitor formed between said pixel electrode and the previous gate line; and,

a second storage capacitor formed between said pixel electrode and said storage capacitor line;

15 wherein a gate-off voltage or a common electrode voltage is applied to said storage capacitor line.

20 10. The liquid crystal display of claim 9, wherein an opening ratio of each pixel at the first pixel row is different from the opening ratio of the pixels at the other pixel rows.

11. The liquid crystal display of claim 10, wherein the opening ratio of the first pixel row is lower than the opening ratio of the other pixel rows.

20 12. The liquid crystal display of claim 11, wherein the difference in the opening ratio is made by differentiating an opening area of said black matrix.

13. The liquid crystal display of claim 12, wherein said black matrix

is formed at said second substrate.

14. The liquid crystal display of claim 13, wherein opening width of said black matrix at the first pixel row in the longitudinal direction of the gate line is identical to opening width of said black matrix at the other pixel rows.

15. The liquid crystal display of claim 13, wherein opening length of said black matrix at the first pixel row in the longitudinal direction of the gate line is shorter than opening length of said black matrix at the other pixel rows.

16. The liquid crystal display of claim 11, wherein a difference in the opening ratio is made by forming a light interception pattern at each pixel of the first pixel row.

17. The liquid crystal display of claim 16, wherein the light interception pattern is formed at the same layer as the data line with the same material.

18. The liquid crystal display of claim 17, wherein the light interception pattern is formed at the same layer as the gate line with the same material.

19. The liquid crystal display of claim 11, wherein the opening ratio of the first pixel row is designed to be 60-80% of the opening ratio of the other pixel rows.

20. The liquid crystal display of claim 9, further comprising a gate-off line formed on said first substrate to transmit a gate-off voltage.

21. The liquid crystal display of claim 20, wherein the gate-off line and said storage capacitor line are formed at the same layer as the gate line.



22. The liquid crystal display of claim 21, wherein the gate-off line and said storage capacitor line are electrically connected to each other via a connection member, and the connection member is formed at the same layer as the data line or said pixel electrode.

5 23. The liquid crystal display of claim 9, further comprising gate signal transmission films arranged at said first substrate and provided with a gate driving integrated circuit that is electrically connected to the gate lines and outputs gate driving signals, and data signal transmission films arranged at said first substrate and provided with a data driving integrated circuit that is electrically connected to the data lines and outputs data driving signals,

10 wherein a common electrode wire for applying the common electrode voltage ( $V_{com}$ ), a gate-on wire for applying the on-voltage  $V_{on}$  to the TFTs controlling the picture signals, a gate-off wire for applying the off-voltage  $V_{off}$ , and wires for transmitting carry-in or gate-clock signals are formed on the edge portion of the first substrate between the gate signal transmission film and the data signal transmission film.

15 24. The liquid crystal display of claim 23, the common electrode wire, the gate-on wire and the gate-off wire are formed at the same layer as the gate lines with the same material.

20 25. A liquid crystal display, comprising:

a first insulating substrate;

a plurality of first signal lines formed on said first substrate;

a first pad connected to an end portion of the first signal line, said first

pad being connected to external driving circuits;

a plurality of second signal lines crossing over the first signal lines to form a pixel area, the pixel area collectively forming a display area;

a second pad connected to an end portion of the second signal line,  
5 said second pad being connected to external driving circuits; and

a first light interception pattern positioned outside of the display area, said first light interception pattern being electrically insulated from the first signal lines and said first pads.

26. The liquid crystal display of claim 25, wherein the first light  
10 interception pattern does not overlap the first signal lines and said first pad.

27. The liquid crystal display of claim 26, wherein the first light interception pattern lies between the display area and said first pad.

28. The liquid crystal display of claim 27, wherein the first light interception pattern is spaced apart from said first pad by a predetermined  
15 distance.

29. The liquid crystal display of claim 25, wherein the first light interception pattern is formed at the same layer as the second signal lines.

30. The liquid crystal display of claim 25, further comprising a second light interception pattern positioned outside of the display area, the  
20 second light interception pattern being electrically insulated from the second signal lines and a second pad.

31. The liquid crystal display of claim 30, wherein the second light interception patterns are formed at the same layer as the first signal lines.

32. The liquid crystal display of claim 25, further comprising a second insulating substrate facing the first insulating substrate.

33. The liquid crystal display of claim 32, further comprising a black matrix defining each pixel area.

5 34. The liquid crystal display of claim 33, wherein the first light interception pattern and the second light interception pattern overlap the black matrix.

35. The liquid crystal display of claim 32, further comprising a sealer that seals the first insulating substrate with the second insulating substrate surrounding the display area.

36. The liquid crystal display of claim 35, wherein the first light interception pattern and the second light interception pattern do not overlap the sealer.

37. The liquid crystal display of claim 32, further comprising a color filter formed on the pixel areas.

38. The liquid crystal display of claim 32, further comprising a common electrode formed on the second insulating substrate.

39. The liquid crystal display of claim 25, further comprising a thin film transistor connected to the first signal line and the second signal line, and a pixel electrode positioned at the pixel areas.

40. A liquid crystal display, comprising:

a first insulating substrate;

a gate line assembly formed at said first insulating substrate, said gate

line assembly comprising a plurality of gate lines, gate electrodes branched from the gate lines, and gate pads connected to the gate lines to transmit scanning signals thereto;

a first light interception pattern isolated from said gate line assembly;

5 a gate insulating layer covering said gate line assembly and said first light interception pattern;

a semiconductor layer formed on said gate insulating layer;

a data line assembly formed on said semiconductor layer and said gate insulating layer, said data line assembly comprising a plurality of data lines crossing over the gate lines while forming pixel areas, source electrodes branched from the data lines, drain electrodes positioned opposite to the source electrodes while centering around the gate electrodes, and data pads connected to the data lines to transmit picture signals thereto, the pixel areas collectively forming a display area;

10 a second light interception pattern isolated from said data line assembly;

a protective layer covering said data line assembly and said second light interception pattern, the protective layer having first to third contact holes exposing the gate pad, the data pad and the drain electrode, respectively; and

20 a pixel electrode connected to the drain electrode via the third contact hole;

wherein said first light interception pattern and said second light interception pattern are positioned outside of the display area.

41. The liquid crystal display of claim 40, wherein said first light interception pattern and said second light interception pattern do not overlap the gate lines and the data lines.

42. The liquid crystal display of claim 40, wherein said first light interception pattern and said second light interception pattern are spaced apart respectively from the gate pads and the data pads by a predetermined distance.

43. The liquid crystal display of claim 40, further comprising:  
a second insulating substrate facing the first substrate;  
a color filter formed at said second substrate corresponding to the pixel areas;  
a black matrix formed at the second substrate surrounding said color filter; and  
a common electrode covering said color filter and said black matrix.

44. The liquid crystal display of claim 43, wherein said first light interception pattern and said second light interception pattern overlap the black matrix.

45. The liquid crystal display of claim 43, further comprising a sealer sealing said first insulating substrate and said second insulating substrate.

46. The liquid crystal display of claim 45, wherein said first light interception pattern and said second light interception pattern do not overlap the sealer.

47. The liquid crystal display of claim 40, further comprising an ohmic contact layer formed on the semiconductor layer.

48. The liquid crystal display of claim 40, further comprising a subsidiary gate pad covering each gate pad via the first contact hole, and a subsidiary data pads covering each data pad via the second contact hole.

49. A method for fabricating a liquid crystal display, comprising the steps of:

forming a gate line assembly and a first light interception pattern on a first insulating substrate such that the first light interception pattern is separated from the gate line assembly;

forming a gate insulating layer such that the gate insulating layer covers the gate line assembly and the first light interception pattern;

forming a semiconductor layer on the gate insulating layer;

forming an ohmic contact layer on the semiconductor layer;

forming a data line assembly and a second light interception pattern such that the data line assembly crosses over the gate line assembly while forming pixel areas and the second light interception patterns are separated from the data line assembly, the pixel areas collectively forming a display area, the first light interception pattern and the second light interception pattern being positioned outside of the display area;

forming a protective layer such that the protective layer covers the data line assembly and the second light interception pattern; and

forming a pixel electrode on the protective layer.

50. The method of claim 49, wherein the first light interception pattern and the second light interception pattern do not overlap the data line assembly and the gate line assembly.

51. The method of claim 49, wherein the semiconductor layer, the ohmic contact layer, the data line assembly, and the second light interception patterns are formed together in one photolithography process.

## **ABSTRACT OF THE DISCLOSURE**

A liquid crystal display includes first and second insulating substrates facing to each other, and a liquid crystal sandwiched between the first and second substrates. A plurality of gate lines are formed at the first substrate to transmit scanning signals, and data lines cross over the gate lines to transmit picture signals. Pads are connected to the gate and data lines. Pixels are demarcated by the gate lines and the data lines, and collectively form a display area. The gate lines demarcate the pixels into rows, and the data lines demarcate the pixels into columns. A black matrix defines each pixel, and a pixel electrode is formed at the pixel. A storage capacitor line is formed at the first substrate parallel to the gate line, and overlapped with the pixel electrodes at the first pixel row. Storage capacitors are formed between the pixel electrodes and the previous gate lines as well as between the pixel electrodes and the storage capacitor line. A gate-off voltage or a common electrode voltage is applied to the storage capacitor line. The opening ratio of each pixel at the first pixel row with the storage capacitor formed between the corresponding pixel electrode and the storage capacitor line differs from the opening ratio of the pixels at the other pixel rows. The difference in the opening ratio is made through forming a light interception pattern at each pixel of the first pixel row, or through differentiating opening areas of the black matrix. In order to prevent leakage of light, light interception patterns may be formed at the region between the display area and the pads.





FIG.2

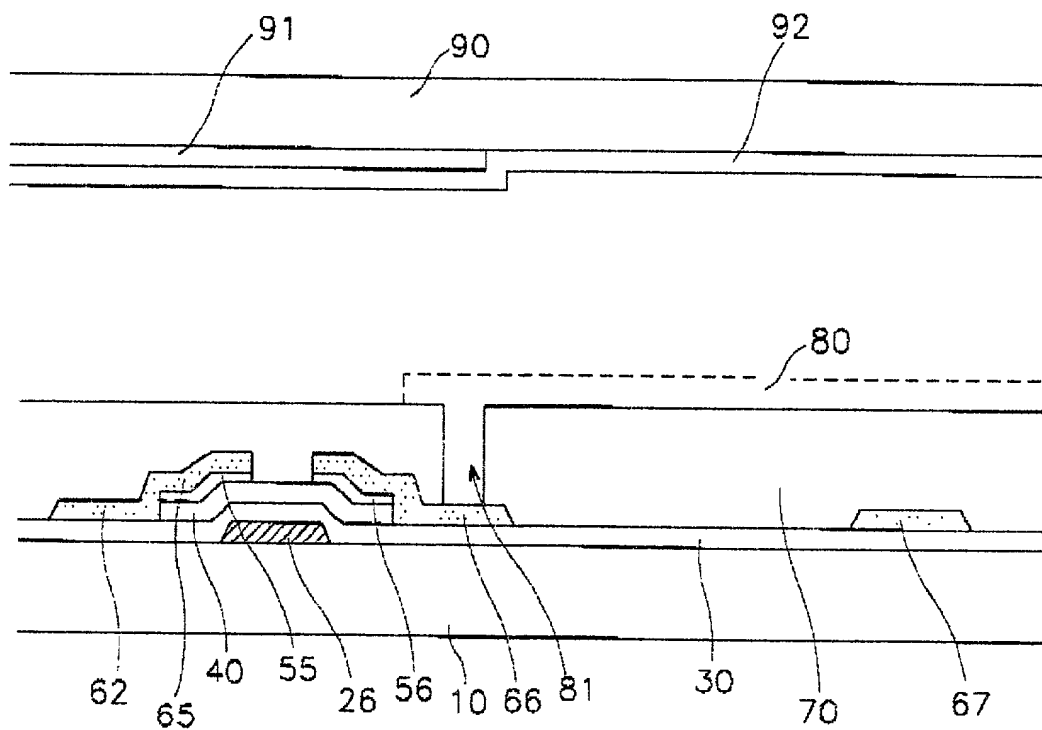


FIG.3

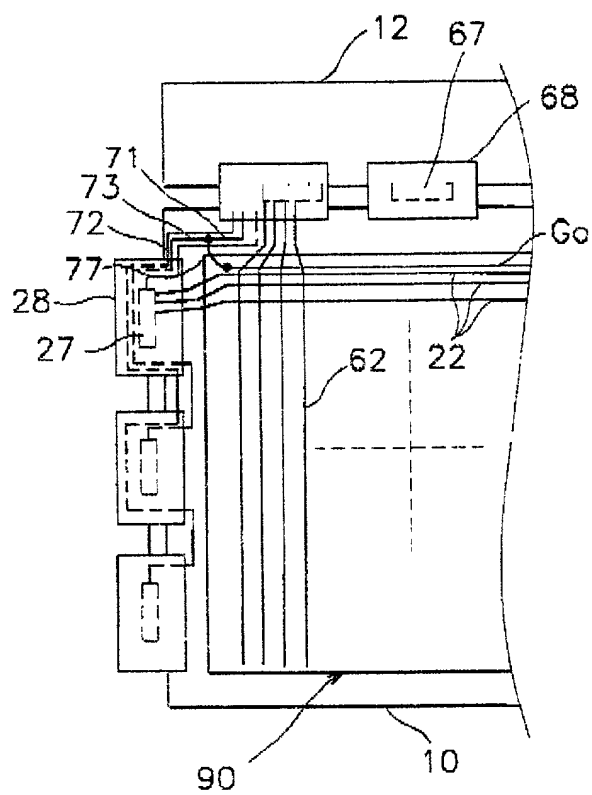
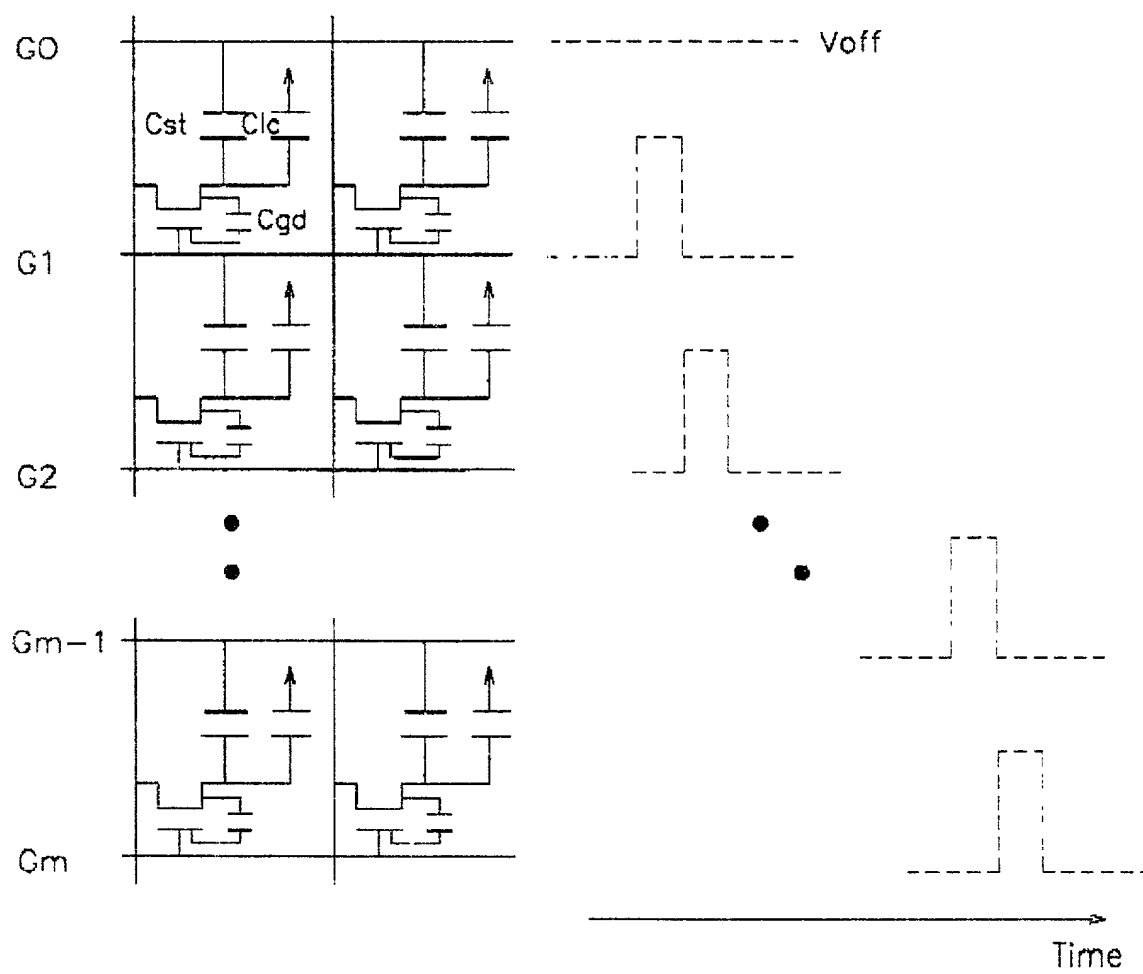


FIG.4



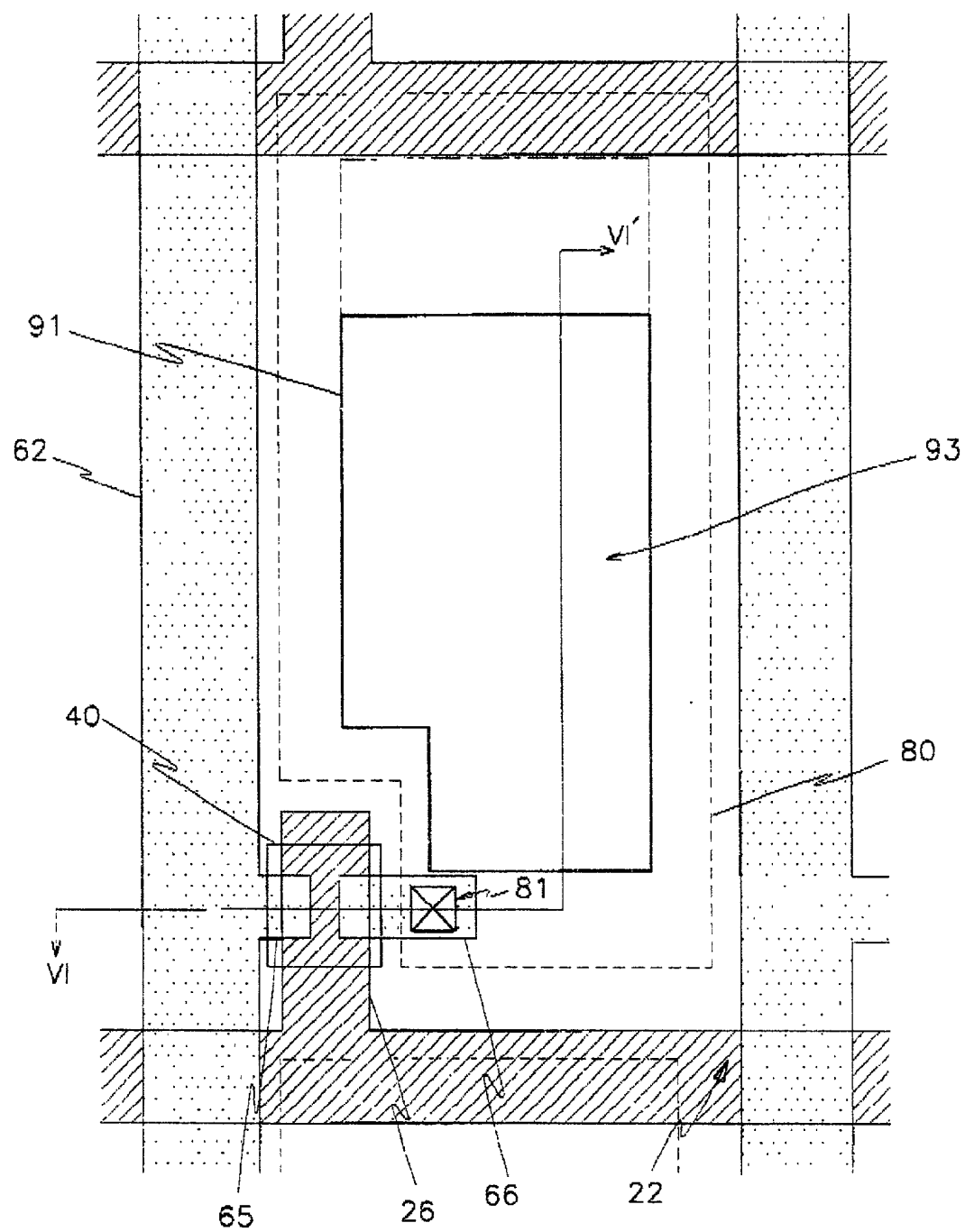


FIG.6

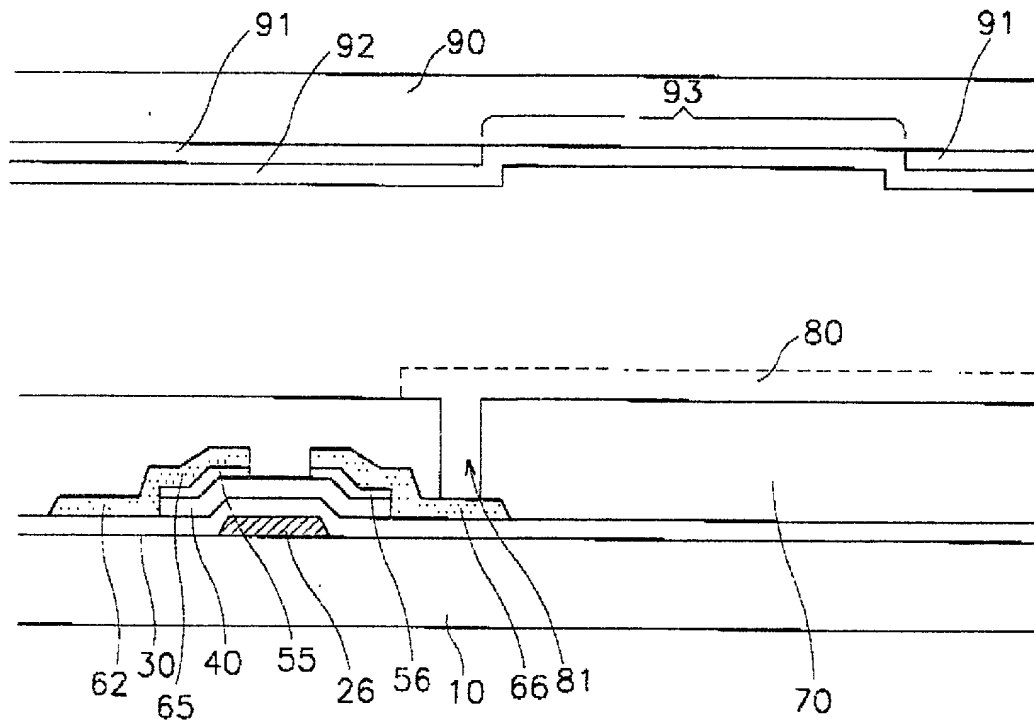


FIG. 7

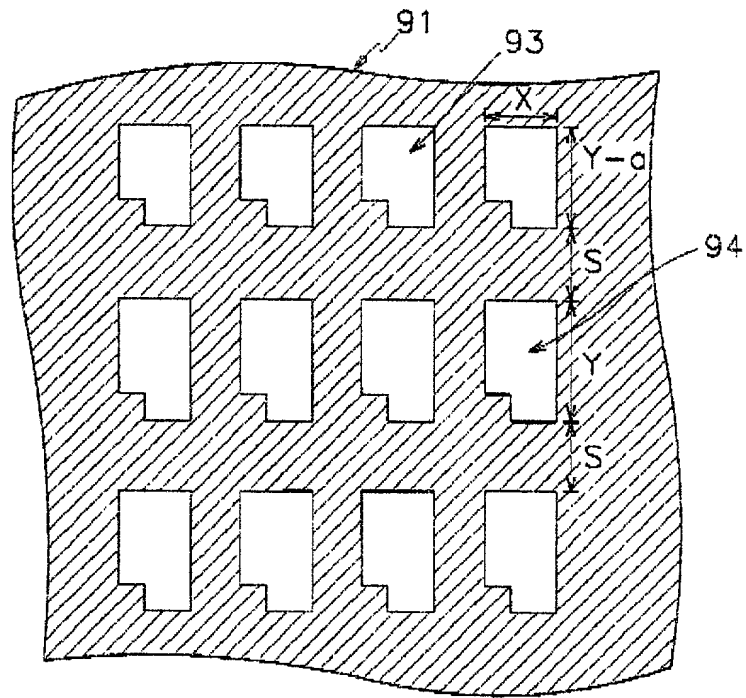
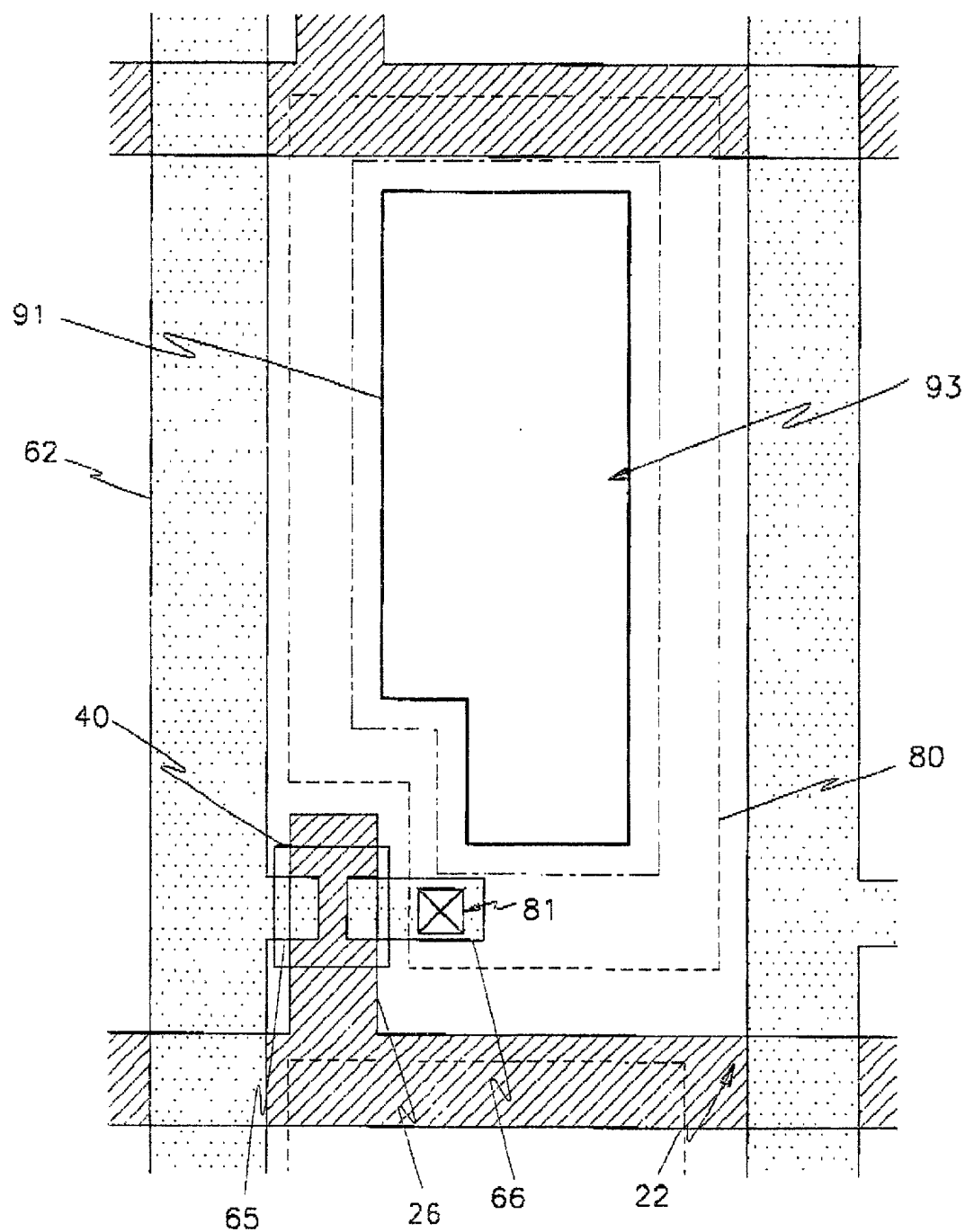


FIG.8





	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095	2096	2097	2098	2099	2100	2101	2102	2103	2104	2105	2106	2107	2108	2109	2110	2111	2112	2113	2114	2115	2116	2117	2118	2119	2120	2121	2122	2123	2124	2125	2126	2127	2128	2129	2130	2131	2132	2133	2134	2135	2136	2137	2138	2139	2140	2141	2142	2143	2144	2145	2146	2147	2148	2149	2150	2151	2152	2153	2154	2155	2156	2157	2158	2159	2160	2161	2162	2163	2164	2165	2166	2167	2168	2169	2170	2171	2172	2173	2174	2175	2176	2177	2178	2179	2180	2181	2182	2183	2184	2185	2186	2187	2188	2189	2190	2191	2192	2193	2194	2195	2196	2197	2198	2199	2200	2201	2202	2203	2204	2205	2206	2207	2208	2209	2210	2211	2212	2213	2214	2215	2216	2217	2218	2219	2220	2221	2222	2223	2224	2225	2226	2227	2228	2229	2230	2231	2232	2233	2234	2235	2236	2237	2238	2239	2240	2241	2242	2243	2244	2245	2246	2247	2248	2249	2250	2251	2252	2253	2254	2255	2256	2257	2258	2259	2260	2261	2262	2263	2264	2265	2266	2267	2268	2269	2270	2271	2272	2273	2274	2275	2276	2277	2278	2279	2280	2281	2282	2283	2284	2285	2286	2287	2288	2289	2290	2291	2292	2293	2294	2295	2296	2297	2298	2299	2300	2301	2302	2303	2304	2305	2306	2307	2308	2309	2310	2311	2312	2313	2314	2315	2316	2317	2318	2319	2320	2321	2322	2323	2324	2325	2326	2327	2328	2329	2330	2331	2332	2333	2334	2335	2336	2337	2338	2339	2340	2341	2342	2343	2344	2345	2346	2347	2348	2349	2350	2351	2352	2353	2354	2355	2356	2357	2358	2359	2360	2361	2362	2363	2364	2365	2366	2367	2368	2369	2370	2371	2372	2373	2374	2375	2376	2377	2378	2379	2380	2381	2382	2383	2384	2385	2386	2387	2388	2389	2390	2391	2392	2393	2394	2395	2396	2397	2398	2399	2400	2401	2402	2403	2404	2405	2406	2407	2408	2409	2410	2411	2412	2413	2414	2415	2416	2417	2418	2419	2420	2421	2422	2423	2424	2425	2426	2427	2428	2429	2430	2431	2432	2433	2434	2435	2436	2437	2438	2439	2440	2441	2442	2
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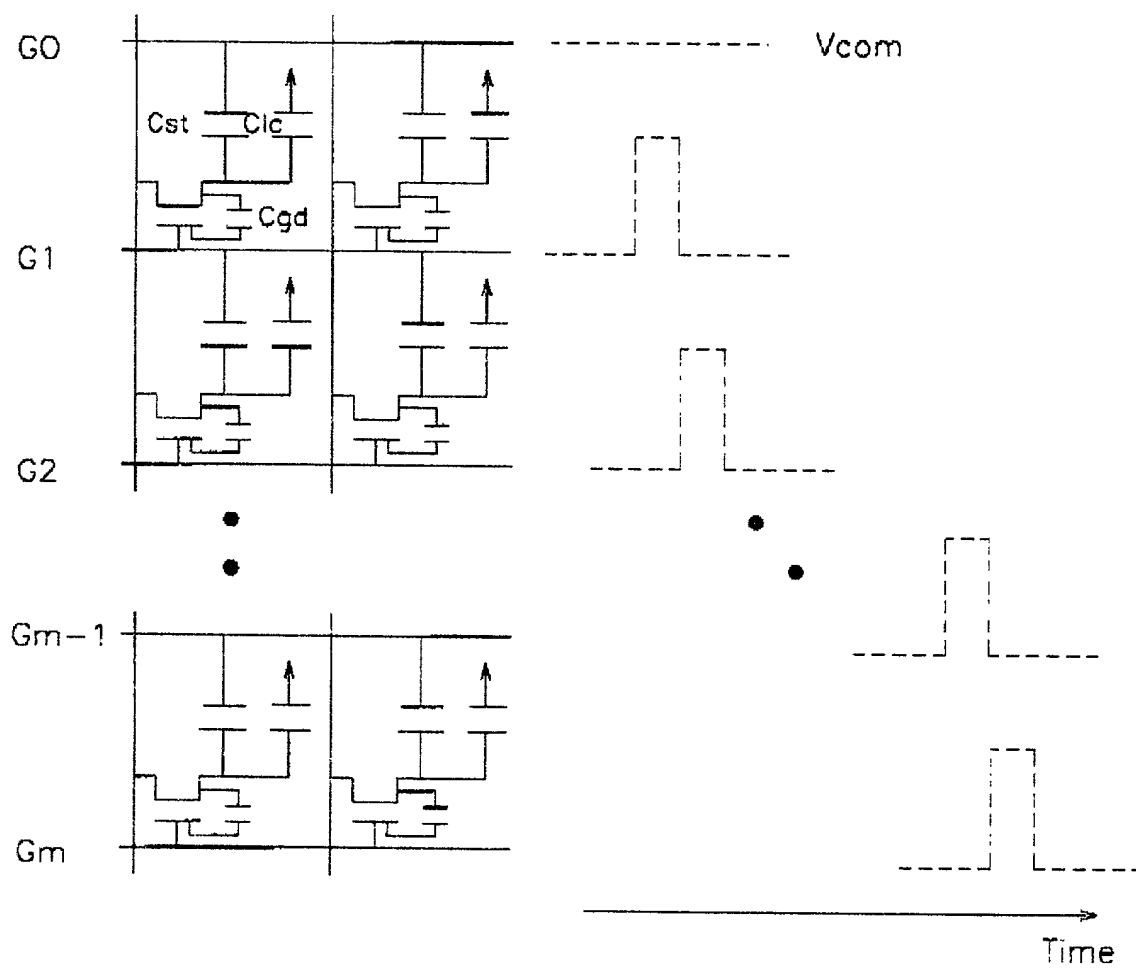


FIG. 10

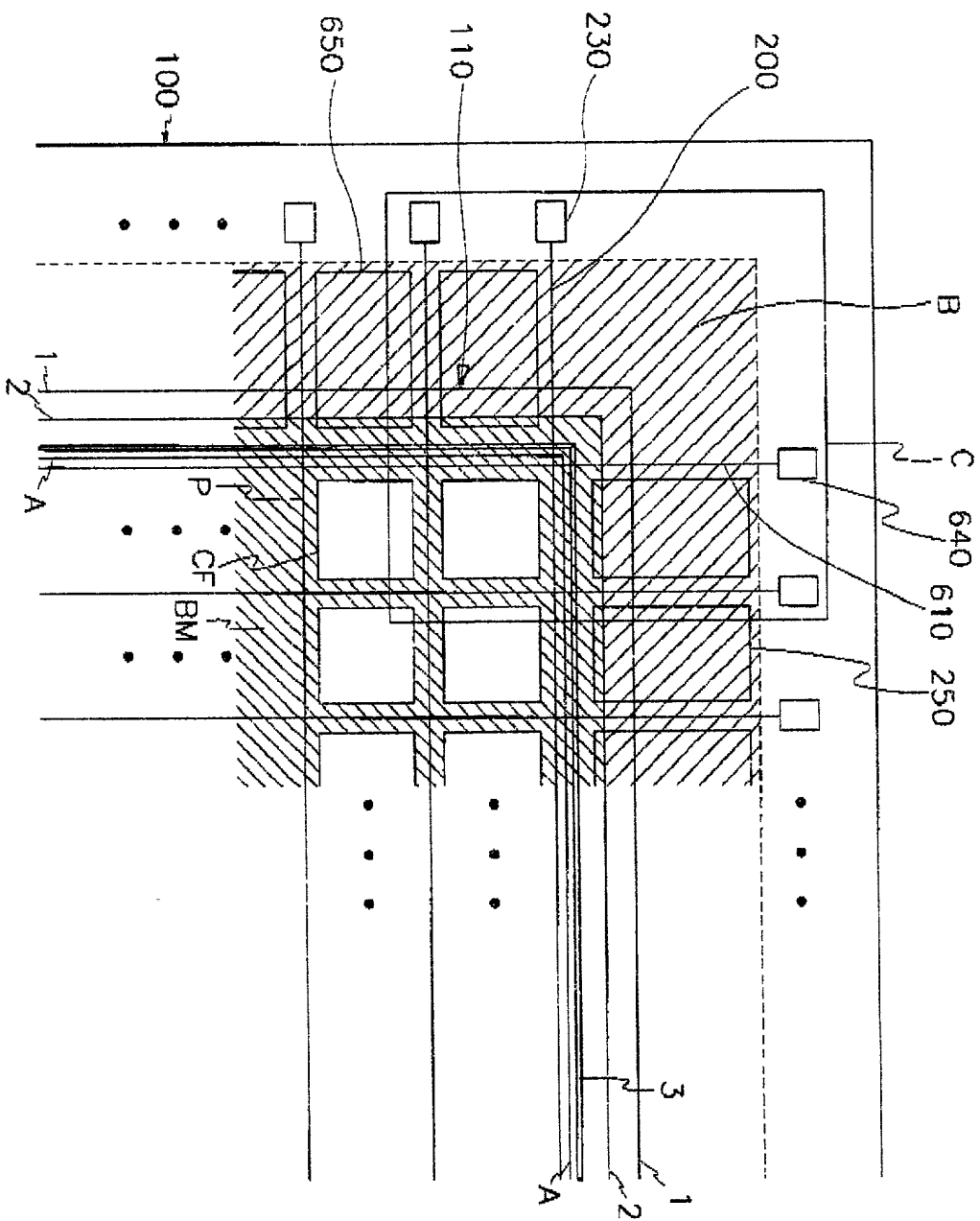


FIG.11

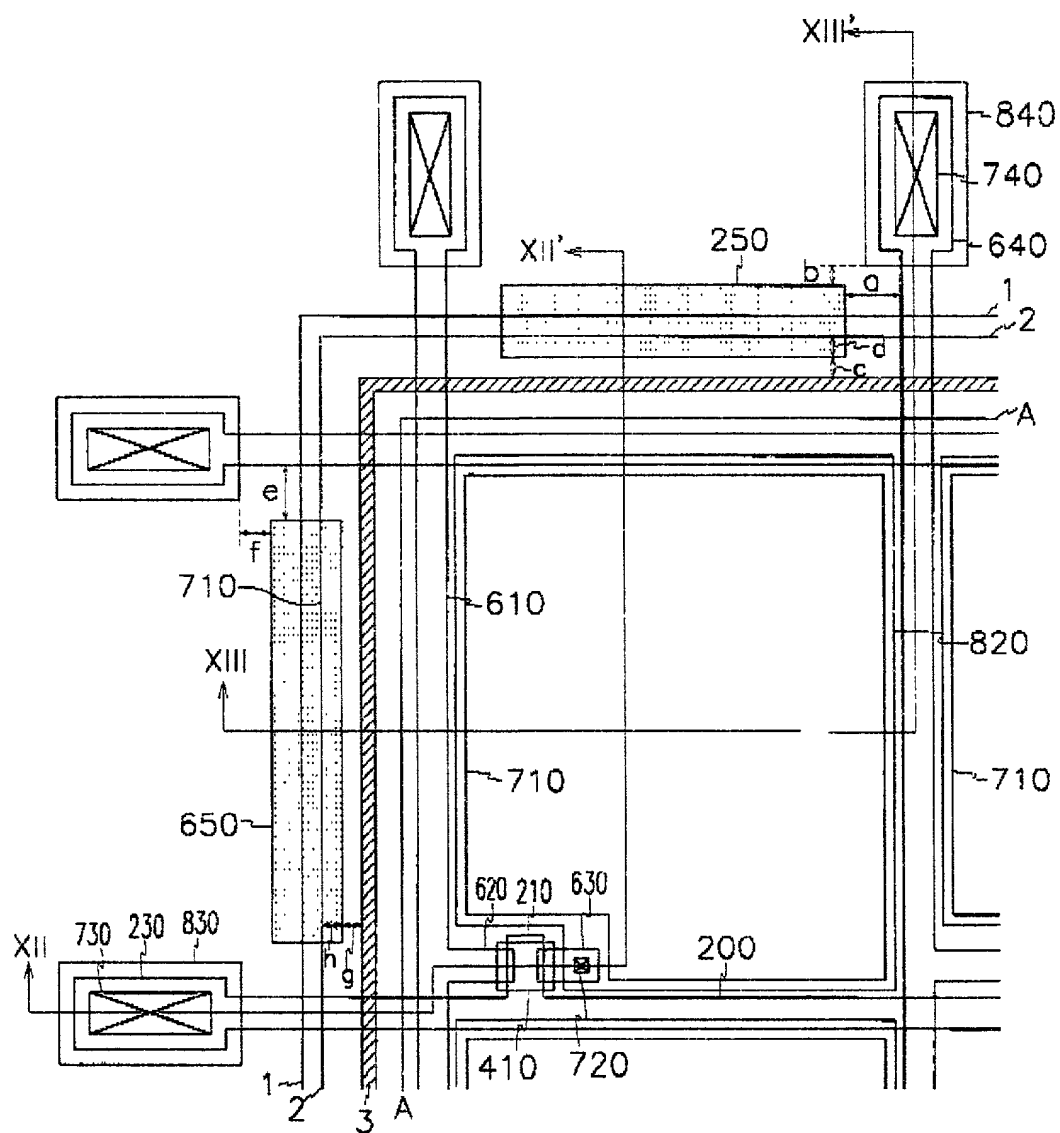


FIG. 12

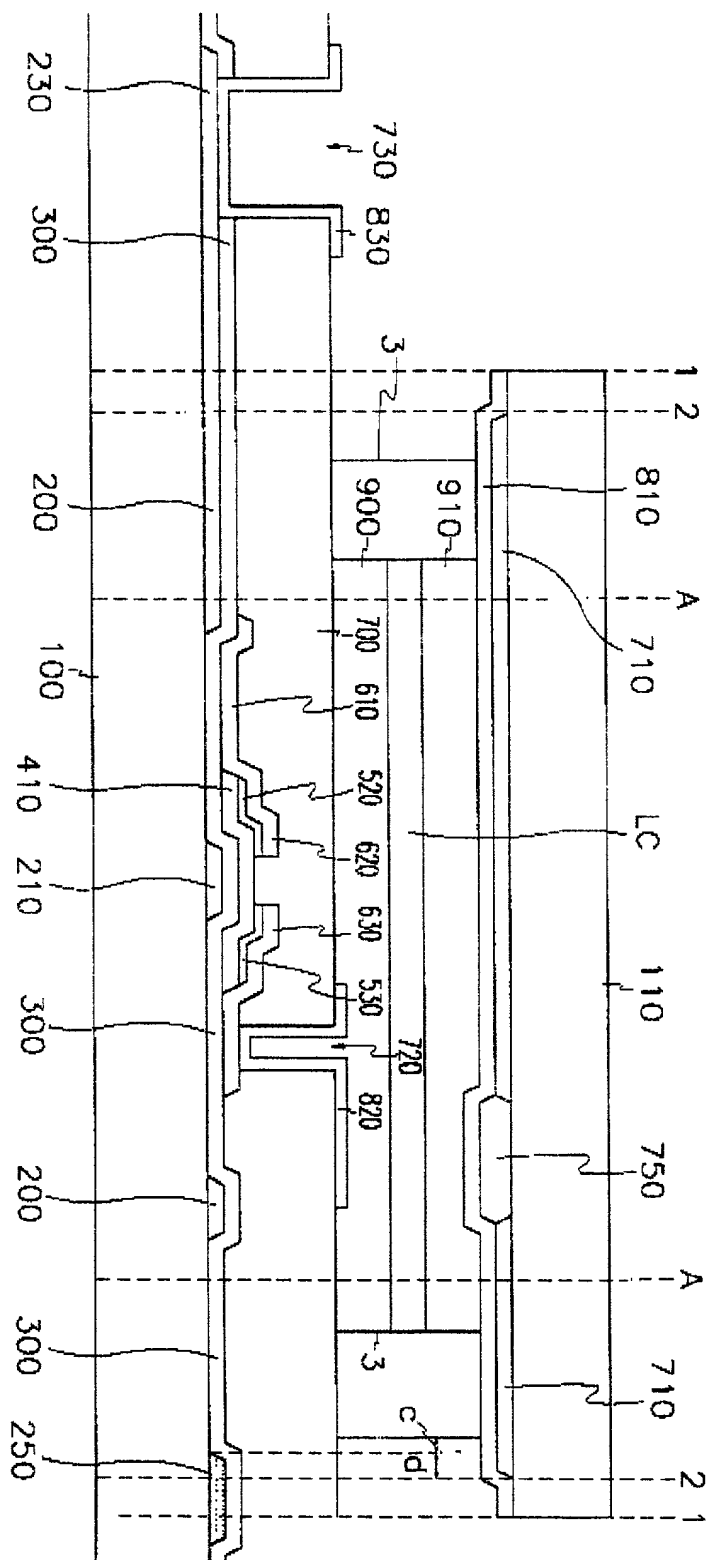


FIG.13

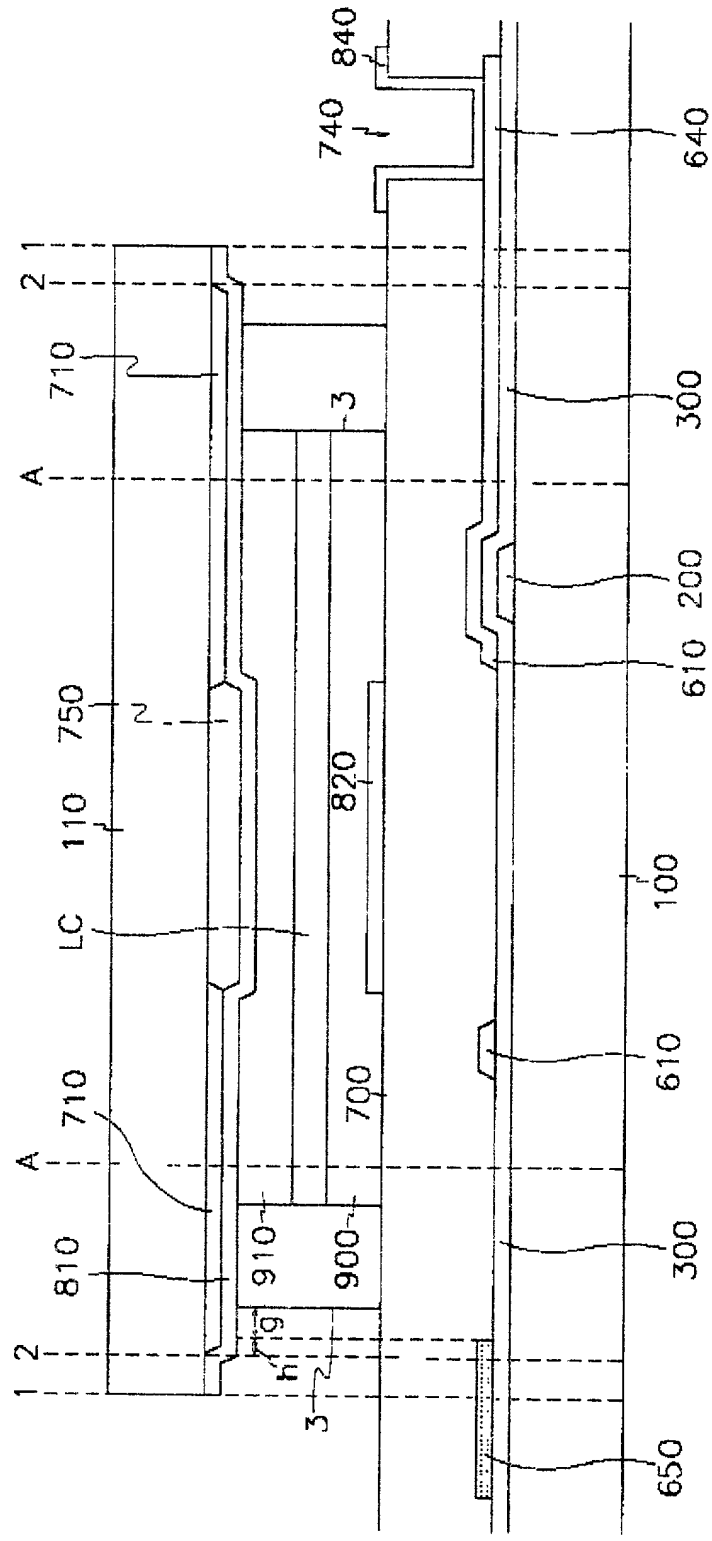


FIG. 14A

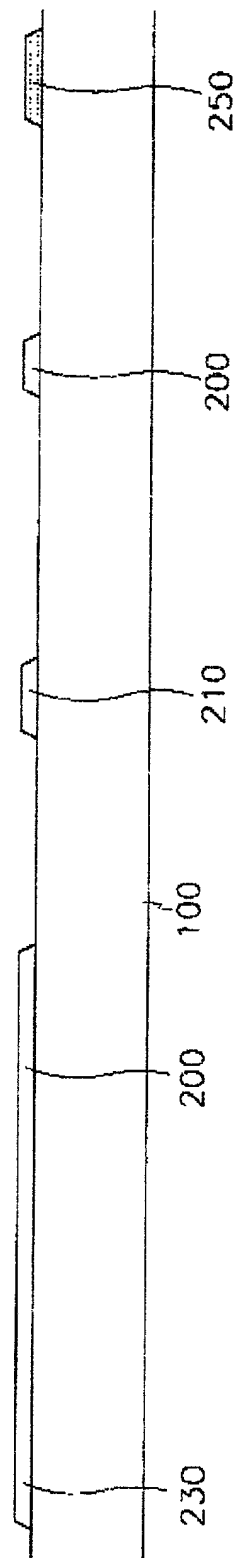


FIG. 14B

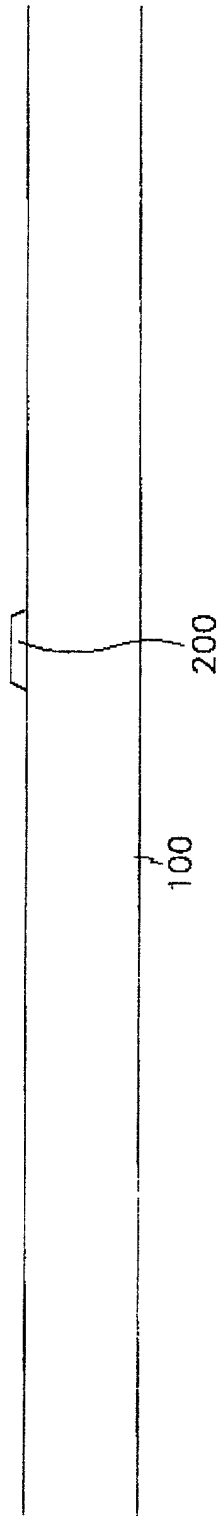


FIG. 15A

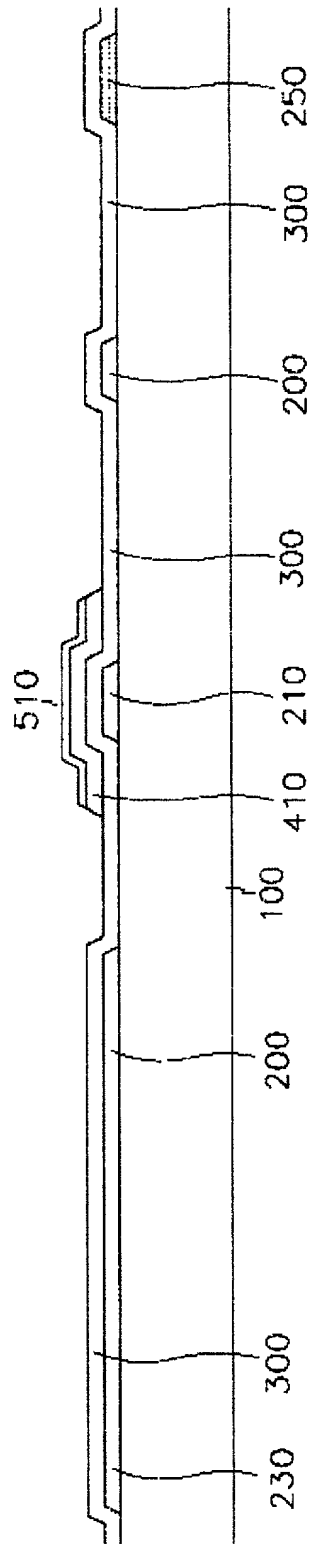




FIG. 15B

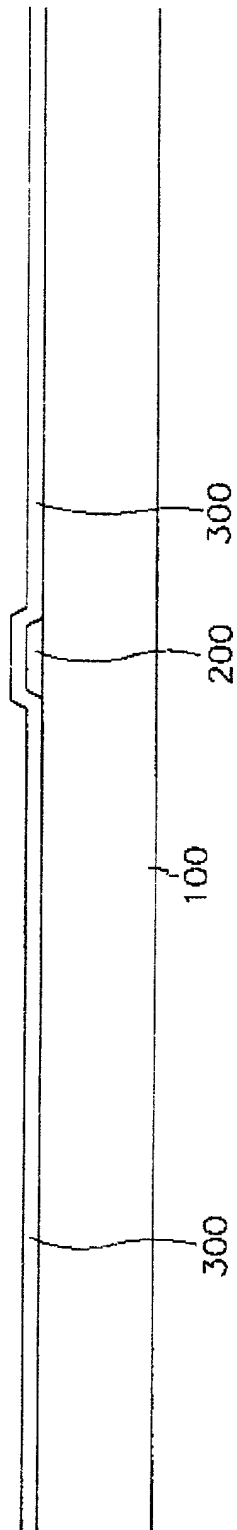


FIG.16A

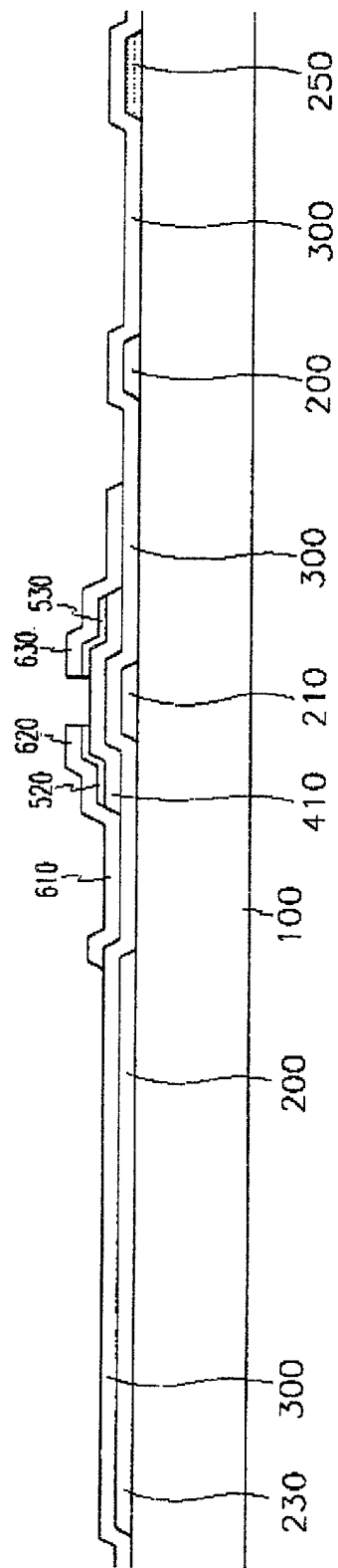


FIG. 16B

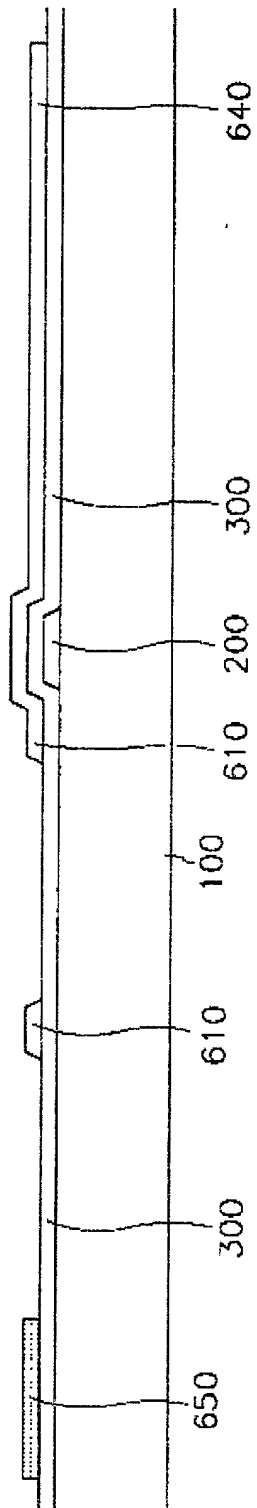




FIG. 17b

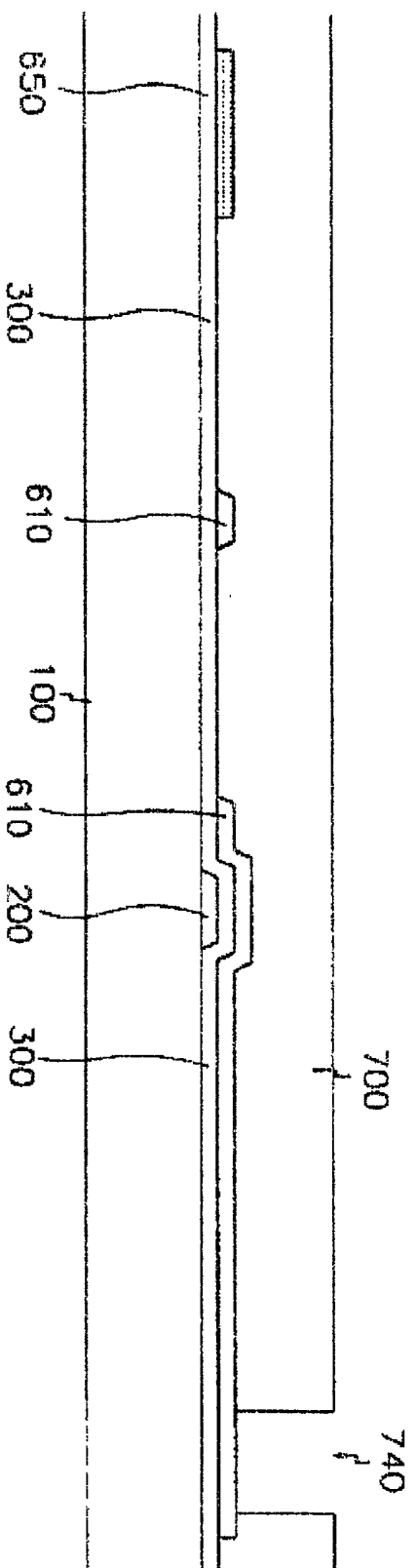


FIG.18

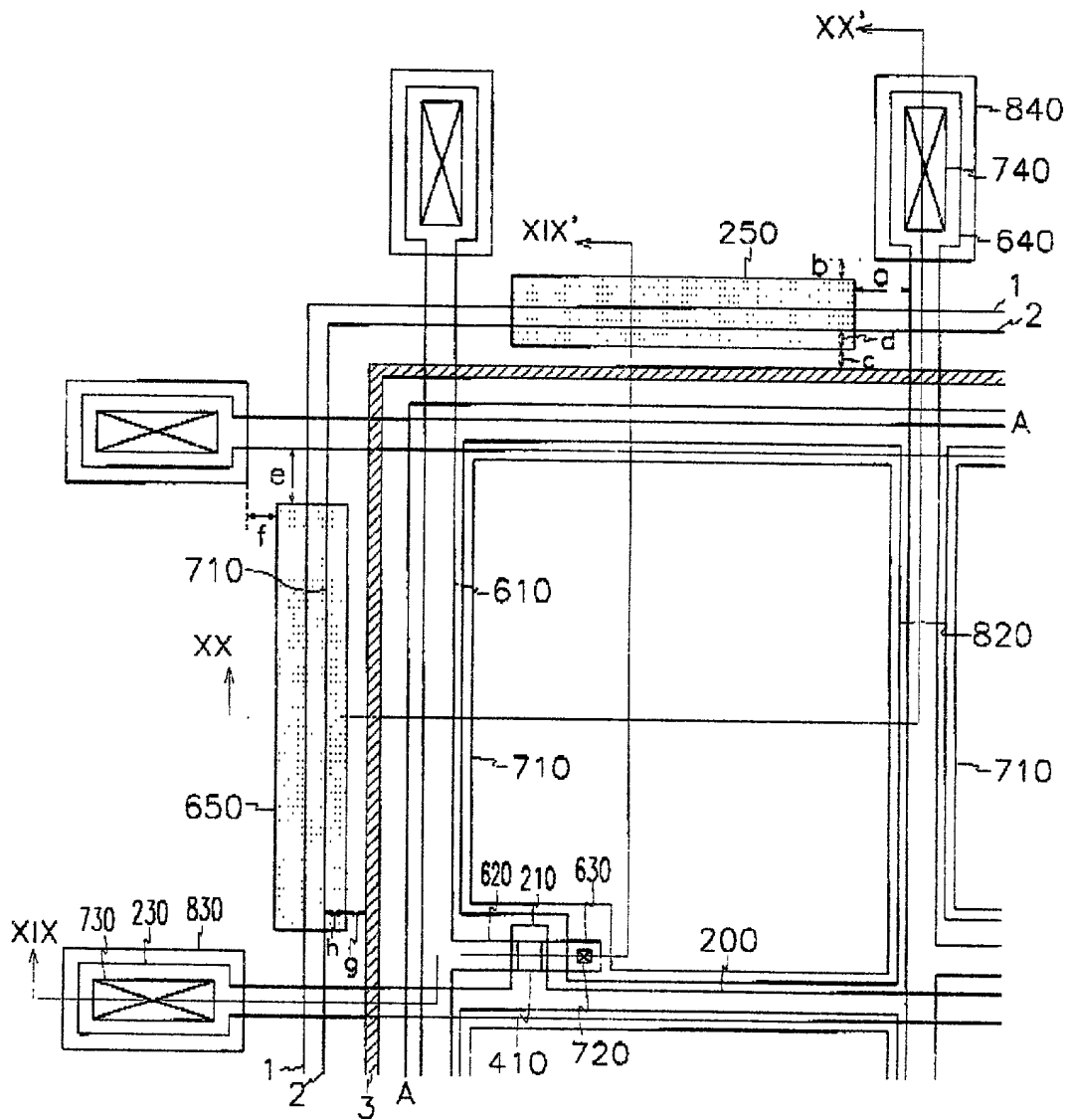


FIG. 19

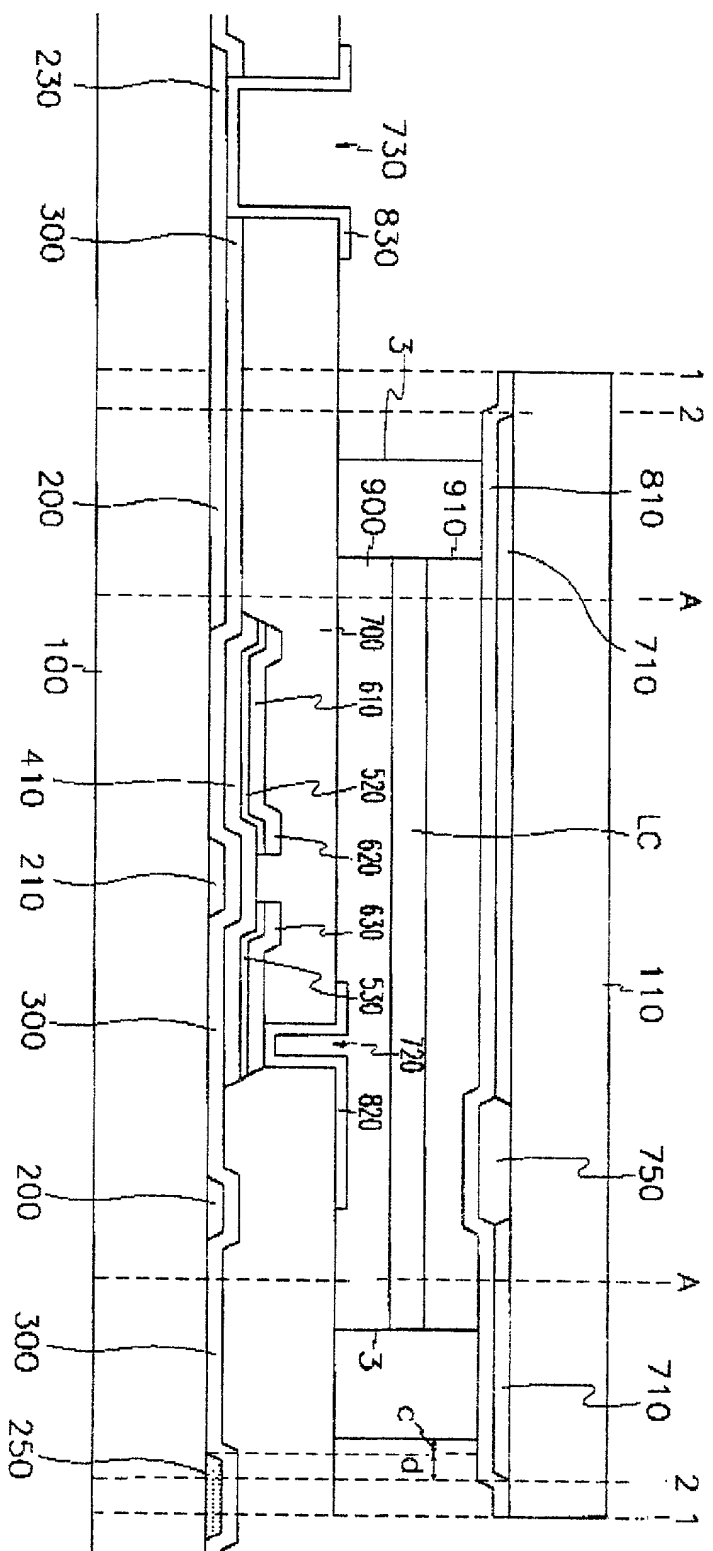


FIG. 20

